Electronics

Higher Technological Institute
Tenth of Ramadan City
Computer science department

Electronics

Author:
A.prof Ahmed Magdy
DR Dina Awny

http://www.hti.edu.eg

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ACKNOWLEDGEMENTS

First before anything I will thank great God (Allah) who gives us the ability to finish this work.

Second, We are extremely grateful to our parents who have sacrificed themselves to give us the best education. From our early childhood, they raised us to love learning, and every one whose supported us to develop our interest in science and engineering. Their unreserved love and support for these many years is what makes this possible. I would also like to thank them for their continuous support, for their patience, encouragement and extra care.

Thank you all.

ABSTRACT

The course description of this course can be summarized and classified to two main branches as the following:

- Electrical part: Basic concepts: SI Units, SI prefixes, charge, current, voltage, power, energy, active elements, and passive elements. Basic laws: ohm's law, conductance, Node, branch, node, Kirchhoff's current law (KCL), Kirchhoff's voltage law (KVL), Series resistance, voltage division, Parallel resistance, and current division. Electrical circuit analysis method and Circuit theorem: Nodal analysis (elimination technique, Cramer's rule, Super node and inspection method for nodal analysis), mesh analysis (Cramer's rule and inspection method for mesh analysis), Superposition, Source transformation, Thevenin's theorem, Norton theorem and Maximum power transfer. Inductors, Capacitors and Transient circuits: Inductors, Capacitors, First order transient circuit (Source free R-C circuit, Forced R-C circuit, Source free R-L circuit and Forced R-L circuit) and Second order transient circuit (R-L-C circuit). Sinusoidal steady state analysis: Phasors and sin wave, Electrical circuit analysis, Circuit theorems and Average and RMS.

- Electronic part: Semiconductors and diode: Material types and properties of semiconductors, Doping process, N-type and P-type, P-N junction, Models for diode and Diode applications (HWR and FWR). Bipolar Junction Transistor (BJT): Basics and fundamentals, Biasing. Field Effect Transistor (FET): Basics and fundamentals, Classification, Biasing. Finally operational Amplifier (OPAMP): Basics and fundamentals, properties of OPAMP and OPAMP applications.

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LIST OF SYMBOLS

A	Ampere
C	Capacitance
D	Diode
E	Energy
I	Electrical current
J	Imaginary
L	Inductance
P	Power
R	Resistance
V	Volt
Ɛ	Permittivity
μ	Mobility
δ	Partial differentiation
φ	Angle

ACRONYMS

Avg	Average
F.B	Forward Bias
FWR	Full Wave Rectifier
HWR	Half Wave Rectifier
KCL	Kirchhoff's Current Law
KVL	Kirchhoff's Voltage Law
RMS	Root Mean Square
R.B	Reverse Bias

CHAPTER 1

CIRCUIT VARIABLES AND ELEMENTS

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CIRCUIT VARIABLES AND ELEMENTS

1.1. Basic concepts

The electrical engineering is one of the most important field. First, we need to understand the basic concepts for electrical circuits.

1.1.1 The international system of units

Here in this subsection, we will state the standard international (SI) units in electrical part in this course as shown in table 1.1.

Table 1.1. SI units

Quantity	Basic unit	Symbol
Time	**Second**	**S**
Length	**Meter**	**M**
Electric current	**Ampere**	**A**
Thermodynamic temperature	**Kelvin**	**K**

1.1.2 The international system of prefixes

As shown in the following table 1.2, the international system of prefixes will be illustrated.

Example 1.1: estimate the following values in V and A.

V_1= 10 KV = 10 * 1000= 10000 V.

V_2= 10 mV = 10/1000 = 0.01 V.

I_1= 20 mA = 20/1000=0.02 A.

I_2= 300 nA= $30*10^{-9}$= 0.0000003 A.

V_3= 1 MV = 1 *10^6= 1000000 V.

Table 1.2. SI prefixes

Multiplier	Prefix	Symbol
10^{18}	**exa**	**E**
10^{15}	**peta**	**P**
10^{12}	**tera**	**T**
10^{9}	**giga**	**G**
10^{6}	**mega**	**M**
10^{3}	**kilo**	**K**
10^{2}	**hecto**	**H**
10^{1}	**deka**	**Da**
10^{-1}	**deci**	**D**
10^{-2}	**centi**	**C**
10^{-3}	**milli**	**M**
10^{-6}	**micro**	**μ**
10^{-9}	**nano**	**N**
10^{-12}	**pico**	**P**
10^{-15}	**femto**	**F**
10^{-18}	**atto**	**A**

1.2. Circuit variables

1.2.1 Electrical charge

The definition of the electrical charge, is an electrical property of the atomic particles of which matter consists, measured in coulombs (C). Its symbols are Q or q(t).

1.2.2 Electrical current

The definition of the electrical current, is the time rate of change of charge, measured in amperes (A). Its symbols are I or i(t). In addition to the relation between electric current and charge is illustrated as the following:

$i = \frac{dq}{dt}$ and $q = \int_{t_0}^{t} i\, dt$ where 1 A= 1 C/s

As shown in figure 1.1, we found two types in electric current. The first one is DC current which is a current that remains constant with time. The second one is AC current which is a current that varies sinusoidal with time.

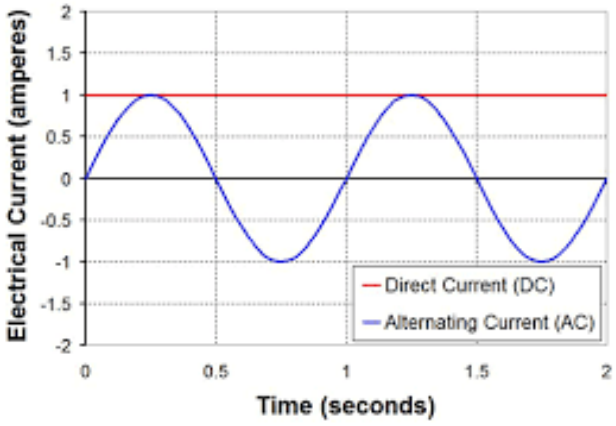


Fig. 1.1: DC and AC electric current

1.2.3 Voltage

The definition of the electrical voltage difference between two points is the energy or work needed to move unit charge from first point to second point, measured in volts (V). Its symbols are V or v(t). In addition to the relation between electric voltage and charge is illustrated as the following:

$v = \frac{dw}{dq}$ where 1 V= 1 J/C.

1.2.4 Power

The definition of the power, is the time rate of expending and absorbing energy, measured in watts (W). Its symbols are P or p(t). In addition to the relation between power and energy is illustrated as the following:

$p = \frac{dw}{dt} = \frac{dw}{dq} * \frac{dq}{dt} = v * i$ where 1 W= 1 J/s.

When the current enters through the positive terminal of an element the relation is p = +vi but if enters through the negative terminal of an element the relation is p = -vi (power absorbed = - power supplied) as shown in figure 1.2.

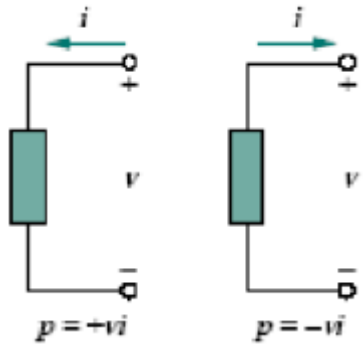


Fig. 1.2: The difference between power absorbed and power supplied

1.2.5 Energy

The definition of the energy, is the capacity to do work, measured in joules (J). Its symbols are W or w(t). In addition to the relation between power and energy is illustrated as the following:

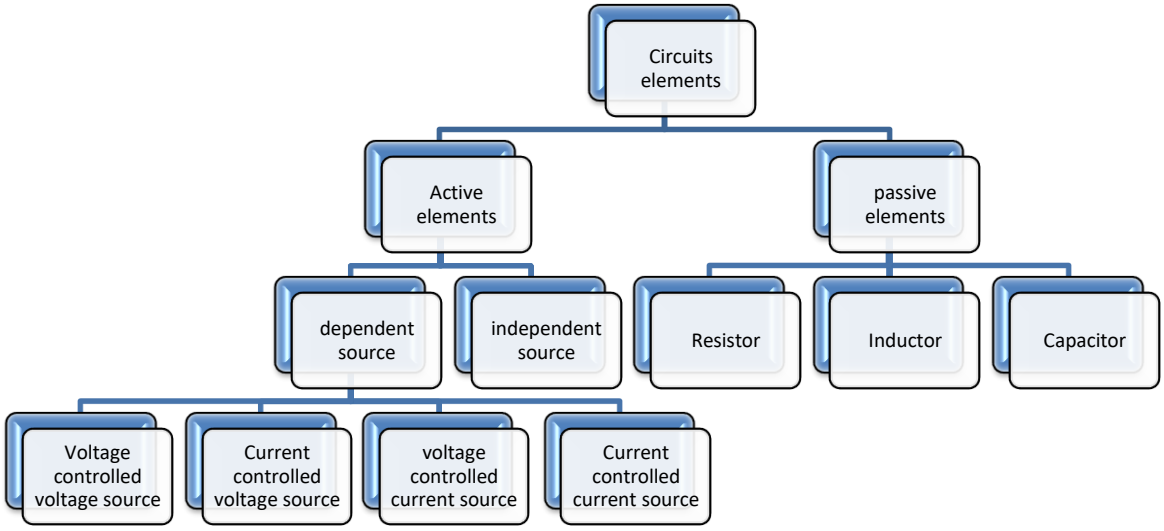
$$w = \int_{t_0}^{t} p\, dt = \int_{t_0}^{t} v * i\, dt$$

Example 1.2: Calculate the energy were consumed in three hours when 200 W electric bulb

w = p*t = 200 * 2 * 3600 = 1440 kJ is the same w = p * t = 200*2 = 400 Wh.

1.3. Circuit elements

Circuit elements are the main parts in any electrical circuits and are classified into two types as the following subsections and figure 1.3:



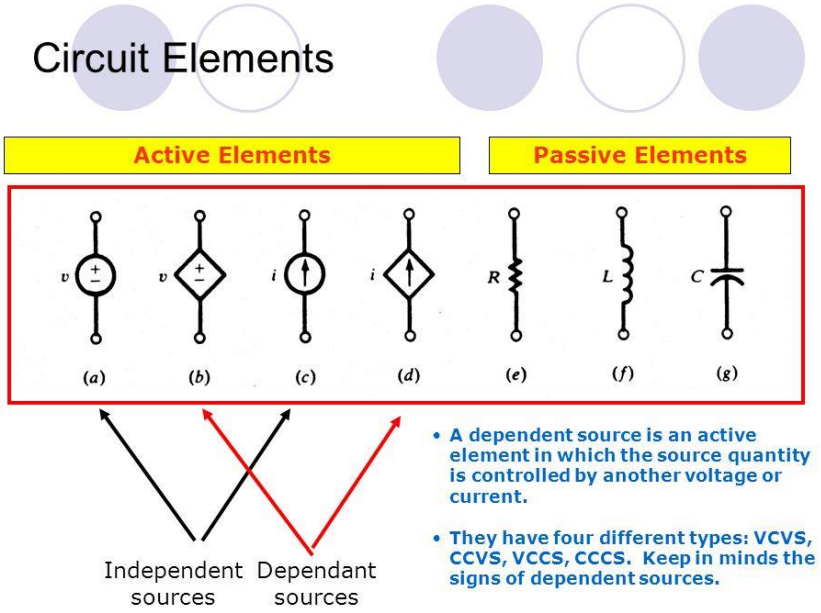


Fig. 1.3: circuit elements

1.3.1 Passive elements

Many components are considered as passive element such as resistor, capacitors, inductors and etc...

1.3.2 Active elements

Many components are considered as active element such as voltage and current source. We can state the four important dependent type:

- voltage controlled voltage source
- current controlled voltage source
- current controlled current source
- voltage controlled current source

1.4. Basic laws and definitions

1.4.1 Ohm's law and conductance

Ohm's law states that the voltage v across a resistor is directly proportional to the current i flowing through the resistor. That is mean v α i where v = i * R. Where the resistance of an element denotes its ability to resist the flow of electrical current, it is measured on ohms (Ω).Where the resistance of any material with a uniform cross-sectional area A depends on A and its length , as shown in figure 1.4. We can represent resistance as measured in the laboratory, in mathematical form R=ρL/A,

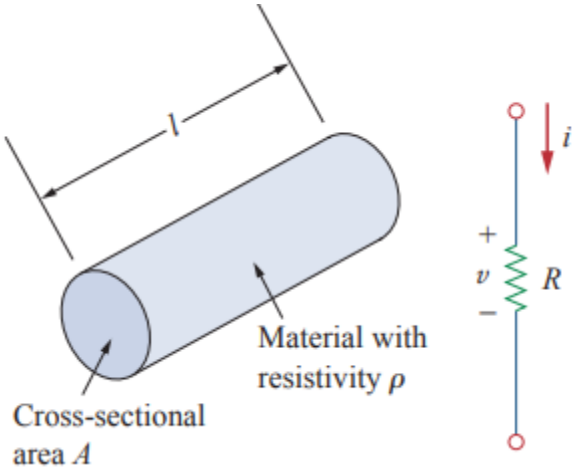


Fig. 1.4: Resistor and its circuit

where ρ is known as the resistivity of the material in ohm-meters. Good conductors, such as copper and aluminum, have low resistivity, while insulators, such as mica and paper, have high resistivity. Table 1.3 presents the values of for some common materials and shows which materials are used for conductors, insulators, and semiconductors. We have special cases asshown in figure 1.5, when an open circuit is

found that is mean R = ∞ and when an short circuit is found that is mean R = 0. On the other hand, conductance is the ability of an element to conduct electrical current, it is measured by moh (ʊ) or Siemens (S) and G = i * v. Now we can say $p = vi = i^2R = v^2/R = v^2G = i^2/G$.

Table 1.3. Some of material resistivity

Materials	Resistivity	Usage
Copper	**$1.72*10^{-8}$**	**Conductor**
Teflon	**$3*10^{12}$**	**Insulators**
Silicon	**$6.4*10^{2}$**	**Semiconductor**
Germanium	**$47*10^{-2}$**	**Semiconductor**

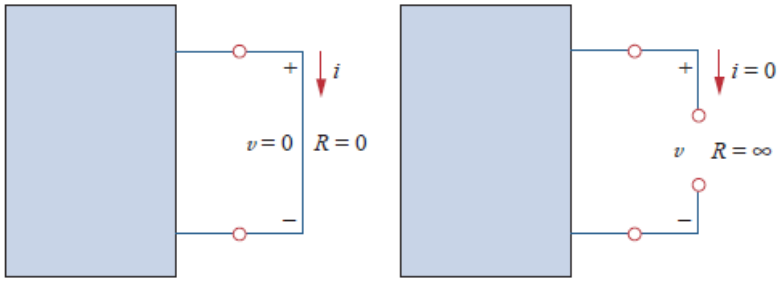
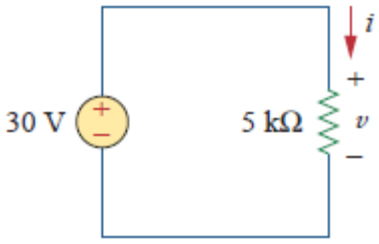


Fig. 1.5: Short circuit and open circuit

Example 1.3: The essential component of a toaster is an electrical element (a resistor) that converts electrical energy to heat energy. How much current is drawn by a toaster with resistance 10 Ω at 110 V?

Answer: 11 A.

Example 1.4: In the circuit shown in the following figure, calculate the current i, the conductance G, and the power p.



Answer:

$i = v/R = 30/5*10^3 = 6$ mA

$G = i/v = 1/R = 0.2$ mS

$P = v*i = 180$ mW

1.4.2 Node, loop and branch

As shown in the figure 1.6, we will present some definitions:

- Branch: represents a single element such as a voltage source or a resistor.
- Node: is a point to connect between two or more branches.
- Loop: is any closed path in the electrical circuit.

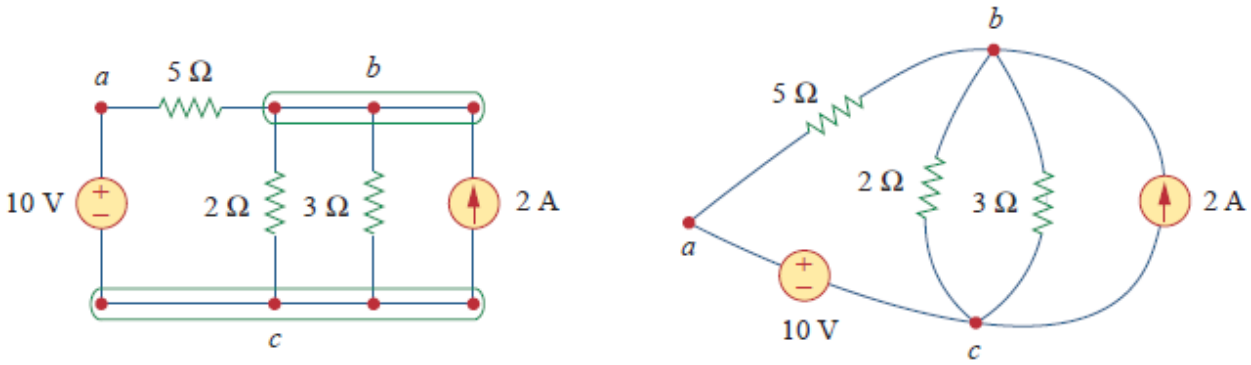
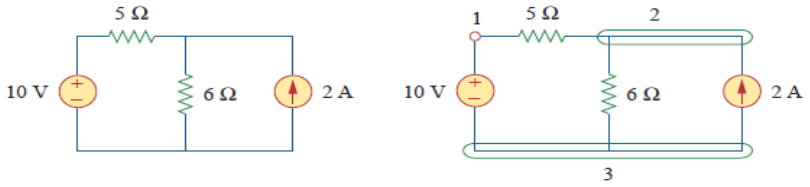
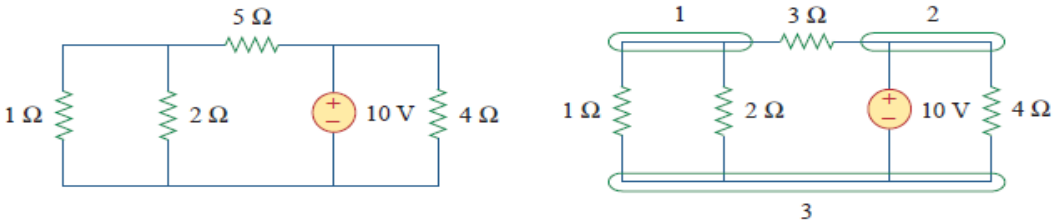


Fig. 1.6: Branch, Node and Loop

Example 1.5: Determine the number of branches and nodes in the circuit shown in the following figures. Identify which elements are in series and which are in parallel.



(a)



(b)

Answer:

(a) Since there are four elements in the circuit, the circuit has four branches: 10 V, 5 Ω, 6Ω, and 2 A. The circuit has three nodes as identified in Fig. (a). The 5Ω resistor is in series with the 10-V voltage source because the same current would flow in both. The 6-resistor is in parallel with the 2-A current source because both are connected to the same nodes 2 and 3.

(b) Five branches and three nodes are identified in Fig. (b). The 1Ω and 2Ω resistors are in parallel. The 4 Ω resistor and 10-V source are also in parallel.

1.5. Sheet 1

1. Determine the current flowing through an element if the charge flow is given by:

$$\text{(a) } q(t) = (3t + 8)\ \text{mC}$$
$$\text{(b) } q(t) = (8t^2 + 4t - 2)\ \text{C}$$
$$\text{(c) } q(t) = (3e^{-t} - 5e^{-2t})\ \text{nC}$$
$$\text{(d) } q(t) = 10 \sin 120\pi t\ \text{pC}$$
$$\text{(e) } q(t) = 20e^{-4t} \cos 50t\ \mu\text{C}$$

2. Find the charge flowing through a device if the current is:

$$\text{(a) } i(t) = 3\ \text{A}, q(0) = 1\ \text{C}$$
$$\text{(b) } i(t) = (2t + 5)\ \text{mA}, q(0) = 0$$
$$\text{(c) } i(t) = 20 \cos(10t + \pi/6)\ \mu\text{A}, q(0) = 2\ \mu\text{C}$$
$$\text{(d) } i(t) = 10e^{-30t} \sin 40t\ \text{A}, q(0) = 0$$

3. A rechargeable flashlight battery is capable of delivering 85 mA for about 12 h. How much charge can it release at that rate? If its terminal voltage is 1.2 V, how much energy can the battery deliver?

4. If the current flowing through an element is given by

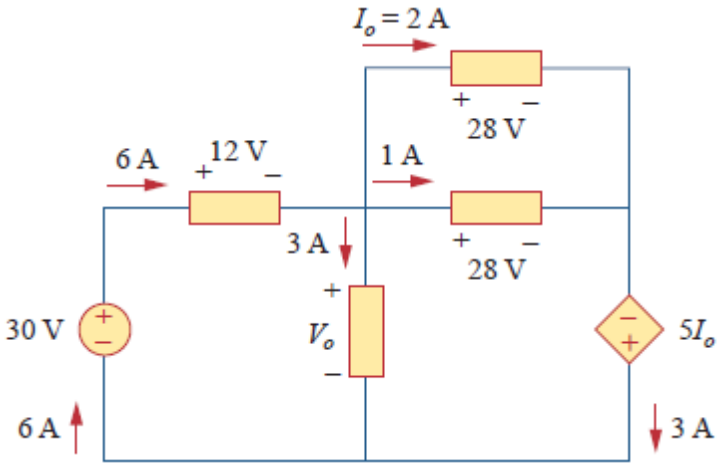
$$i(t) = \begin{cases} 3t\text{A}, & 0 \leqq t < 6\ \text{s} \\ 18\text{A}, & 6 \leqq t < 10\ \text{s} \\ -12\text{A}, & 10 \leqq t < 15\ \text{s} \\ 0, & t \geqq 15\ \text{s} \end{cases}$$

   Plot the charge stored in the element over $0 < t < 20$ s.

5. The current entering the positive terminal of a device is $i(t) = 3\ e^{-2t}$ A and the voltage across the device is $v(t) = 5\ di/dt$ V.

   (a) Find the charge delivered to the device between t = 0 and t = 2 s.
   (b) Calculate the power absorbed.
   (c) Determine the energy absorbed in 3 s.

6. Find V_o in the circuit of the following figure



7. An electric stove with four burners and an oven is used in preparing a meal as follows.

   Burner 1: 20 minutes Burner 2: 40 minutes
   Burner 3: 15 minutes Burner 4: 45 minutes
   Oven: 30 minutes

   If each burner is rated at 1.2 kW and the oven at 1.8 kW, and electricity costs 12 cents per kWh, calculate the cost of electricity used in preparing the meal.

8. Find the power rating of the following electrical appliances in your household:
   (a) Light bulb (b) Radio set
   (c) TV set (d) Refrigerator
   (e) Personal computer (f) PC printer
   (g) Microwave oven (h) Blender

9. A 1.5-kW electric heater is connected to a 120-V source.

   (a) How much current does the heater draw?
   (b) If the heater is on for 45 minutes, how much energy is consumed in kilowatt-hours (kWh)?
   (c) Calculate the cost of operating the heater for 45 minutes if energy costs 10 cents/kWh.

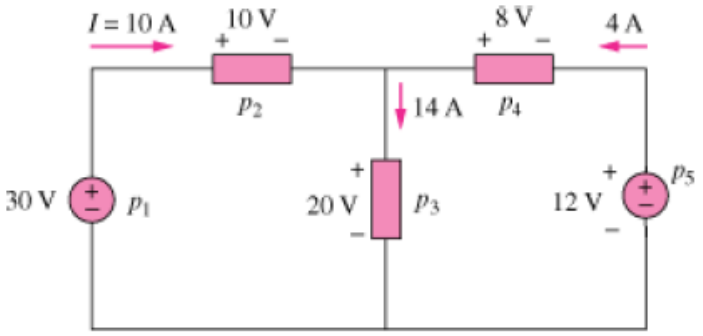
10. A flashlight battery has a rating of 0.8 ampere-hours (Ah) and a lifetime of 10 hours.

    (a) How much current can it deliver?
    (b)How much power can it give if its terminal voltage is 6 V?
    (c) How much energy is stored in the battery in kWh?

11. GPU Energy (the electric power company in New Jersey) charged a consumer $52.75 one month. If the basic service charge is $5.23 and the company charges $0.11 per kWh, how much energy in kWh was used by the consumer?

12. How much energy does a 10-hp motor deliver in 30 minutes? Assume that 1 horse power = 746 W.

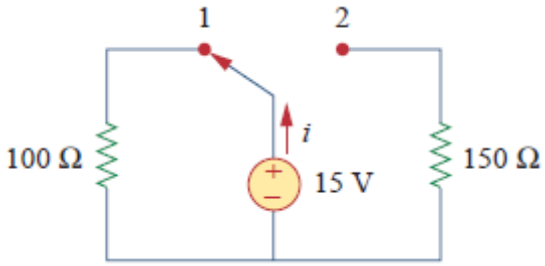
13. Find the power absorbed by each of the elements in the following figure:



14. The voltage across a 5-kΩ resistor is 16 V. Find the current through the resistor.

15. Find the hot resistance of a lightbulb rated 60 W, 120 V.

16. When the voltage across a resistor is 120 V, the current through it is 2.5 mA. Calculate its conductance.
    (a) Calculate current i in the following figure when the switch is in position 1.
    (b) Find the current when the switch is in position 2.



CHAPTER 2

TECHNIQUES OF CIRCUIT ANALYSIS

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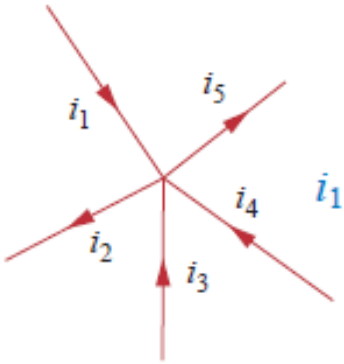
2.1 Kirchhoff's current and voltage law

In Kirchhoff's current law (KCL) states that the algebraic sum of currents entering a node (or a closed boundary) is zero. Mathematically, KCL implies that

$$\sum_{n=1}^{N} i_n = 0$$

where N is the number of branches connected to the node and i_n is the n-th current entering (or leaving) the node. As shown in figure 2.1, by this law, currents entering a node may be regarded as positive, while currents leaving the node may be taken as negative or vice versa.



$$i_1 + (-i_2) + i_3 + i_4 + (-i_5) = 0$$

Fig. 2.1: Example on KCL

As shown in figure 2.2, the sum of the currents entering a node is equal to the sum of the currents leaving the node.

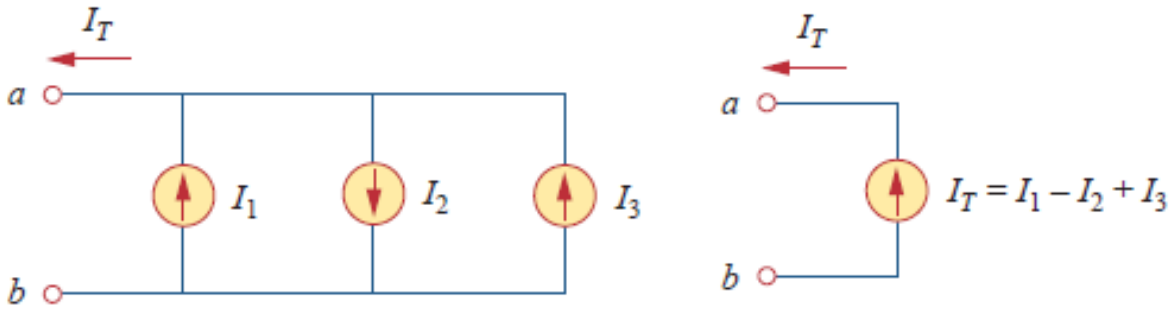
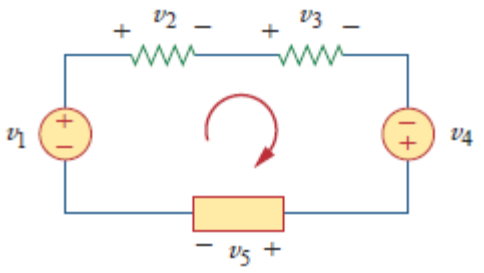


Fig. 2.2: Another example on KCL

In Kirchhoff's voltage law (KVL) states that the algebraic sum of all voltages around a closed path (or loop) is zero. Mathematically, KVL implies that

$$\sum_{m=1}^{M} v_m = 0$$

where M is the number of voltages in the loop (or the number of branches in the loop) and v_m is the m-th voltage. As shown in figure 2.3, by this law, The sign on each voltage is the polarity of the terminal encountered first as we travel around the loop. We can start with any branch and go around the loop either clockwise or counterclockwise. In other words, sum of voltage drops = sum of voltage rises

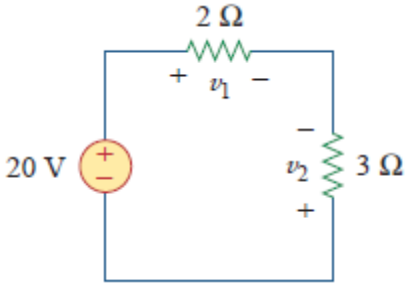


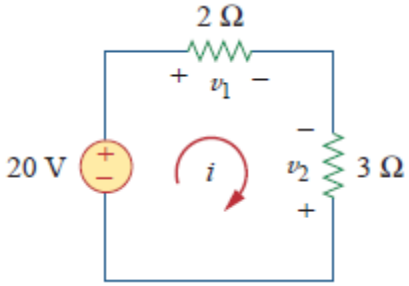
$$-v_1 + v_2 + v_3 - v_4 + v_5 = 0$$

$$v_2 + v_3 + v_5 = v_1 + v_4$$

Fig. 2.3: Example on KVL

Example 2.1: For the circuit in the following figure, find voltages v_1 and v_2.





Answer: To find v_1 and v_2 we apply Ohm's law and Kirchhoff's voltage law. Assume that current *i* flows through the loop as shown in Fig.. From Ohm's law,

$$v_1=2i, \qquad v_2 = -3i.$$

Applying KVL around the loop gives

$$-20 + v_1 - v_2 = 0$$

we obtain i = 4 A.

$$v_1= 8 \text{ V and } v_2 = -12 \text{ V}$$

2.2 Series and parallel resistance

The process of combining the resistors is facilitated by combining two of them at a time. With this in mind, consider the single-loop circuit of figure 2.4. The two resistors are in series, since the same current i flows in both of them. Applying Ohm's law to each of the resistors, we obtain

$$v_1 = i\,R_1 \text{ and } v_2 = i\,R_2$$

$$-v + v_1 + v_2 = 0$$

$$v = v_1 + v_2 = i(R_1 + R_2)$$

$$i = \frac{v}{(R_1 + R_2)}$$

$$v = i\,R_{eq}$$

$$R_{eq} = R_1 + R_2$$

Now we can say The equivalent resistance of any number of resistors connected in series is the sum of the individual resistances.

$$R_{eq} = \sum_{i=1}^{N} R_i$$

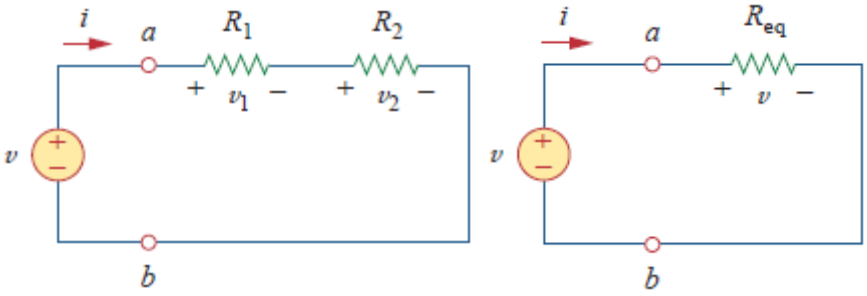


Fig. 2.4: A single-loop circuit with two resistors in series.

If $R_1 = R_2 = \cdots = R_N = R$, then

$$R_{eq} = NR$$

where two resistors are connected in parallel and therefore have the same voltage across them as shown in figure 2.5. From Ohm's law,

$$v = iR_1 = iR_2$$

$$i_1 = \frac{v}{R_1}, \qquad i_2 = \frac{v}{R_2}$$

$$i = i_1 + i_2 = \frac{v}{R_1} + \frac{v}{R_2} = v\left(\frac{1}{R_1} + \frac{1}{R_2}\right) = \frac{v}{R_{eq}}$$

$$\frac{1}{R_{eq}} = \frac{1}{R_1} + \frac{1}{R_2}$$

$$R_{eq} = \frac{R_1 R_2}{R_1 + R_2}$$

$$\frac{1}{R_{eq}} = \frac{1}{R_1} + \frac{1}{R_2} + \cdots + \frac{1}{R_N}$$

The equivalent resistance of two parallel resistors is equal to the product of their resistances divided by their sum.

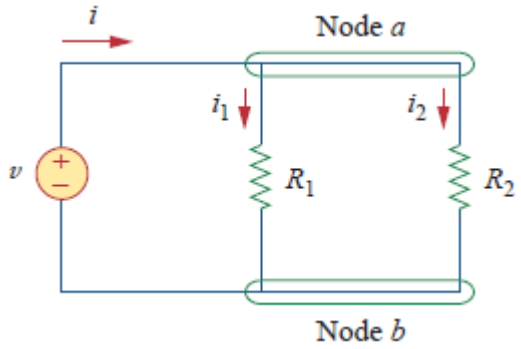


Fig. 2.5: A single-loop circuit with two resistors in parallel.

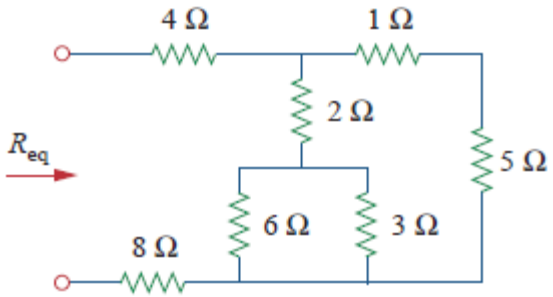
Note that the equivalent resistance is always smaller than the resistance of the smallest resistor in the parallel combination. If $R_1 = R_2 = \cdots = R_N = R$, then

$$R_{eq} = \frac{R}{N}$$

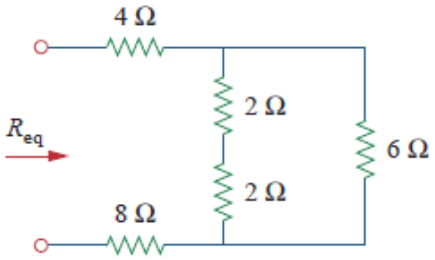
The equivalent conductance of resistors connected in parallel is the sum of their individual conductance.

$$G_{eq} = G_1 + G_2 + \cdots + G_N$$

Example 2.2: Find R_{eq} for the circuit shown in the following figure



Answer:

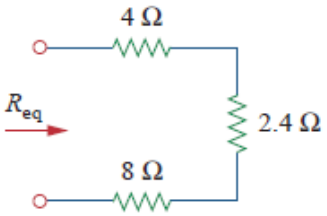


Two resistors 6 and 3 parallel

6 // 3 = 2 Ω

Two resistors 2 and 2 series and parallel with 6

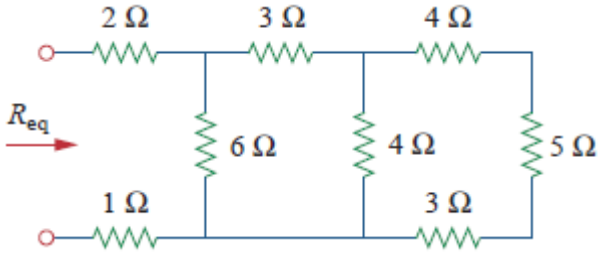
(2+2) // 6 = 2.4 Ω



Three resistances 4, 8 and 2.4 are series

4 + 8 + 2.4 = 14.4 Ω

Example 2.3: Find R_{eq} for the circuit shown in the following figure



Answer: 6 Ω.

2.3 Voltage and current division

To determine the voltage across each resistor by using voltage divider in figure 2.4 as the following

$$v_1 = \frac{R_1}{(R_1+R_2)}v \qquad v_2 = \frac{R_2}{(R_1+R_2)}v$$

$$v_i = \frac{R_i}{(R_1 + R_2 + \ldots\ldots + R_N)}v$$

To determine the current through each resistor by using current divider in figure 2.5 as the following

$$v = iR_{eq} = \frac{iR_1R_2}{(R_1 + R_2)} = i_1R_1 = i_2R_2$$

$$i_1 = \frac{R_2}{(R_1 + R_2)}i$$

$$i_2 = \frac{R_1}{(R_1 + R_2)} i$$

2.4 Nodal analysis

Nodal analysis provides a general procedure for analyzing circuits using node voltages as the circuit variables. Choosing node voltages instead of element voltages as circuit variables is convenient and reduces the number of equations one must solve simultaneously. To simplify matters, we shall assume in this section that circuits do not contain voltage sources. Circuits that contain voltage sources will be analyzed in the next section. In nodal analysis, we are interested in finding the node voltages. Given a circuit with n nodes without voltage sources, the nodal analysis of the circuit involves taking the following three steps.

- Select a node as the reference node as shown in figure 2.6. Assign voltages $v_1, v_2, \ldots, v_n$ to the remaining (n-1) nodes. The voltages are referenced with respect to the reference node.
- Apply KCL to each of the (n-1) non-reference nodes. Use Ohm's law to express the branch currents in terms of node voltages.
- Solve the resulting simultaneous equations to obtain the unknown node voltages.

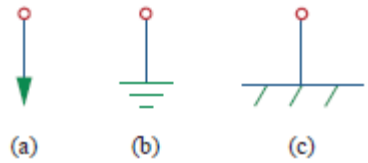


Fig. 2.6: Symbols of references node.

As shown in figure 2.7, Current flows from a higher potential to a lower potential in a resistor.

$$i = \frac{v_{higher} - v_{lower}}{R}$$

$$i_1 = \frac{v_1 - 0}{R_1} = G_1 v_1$$

$$i_2 = \frac{v_1 - v_2}{R_2} = G_2(v_1 - v_2)$$

$$i_3 = \frac{v_2 - 0}{R_3} = G_3 v_2$$

node 1:

$$I_1 = I_2 + \frac{v_1}{R_1} + \frac{v_1 - v_2}{R_2}$$

node 2:

$$\frac{v_2}{R_3} = I_2 + \frac{v_1 - v_2}{R_2}$$

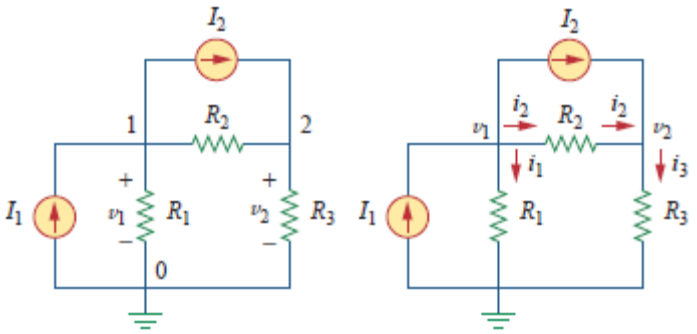
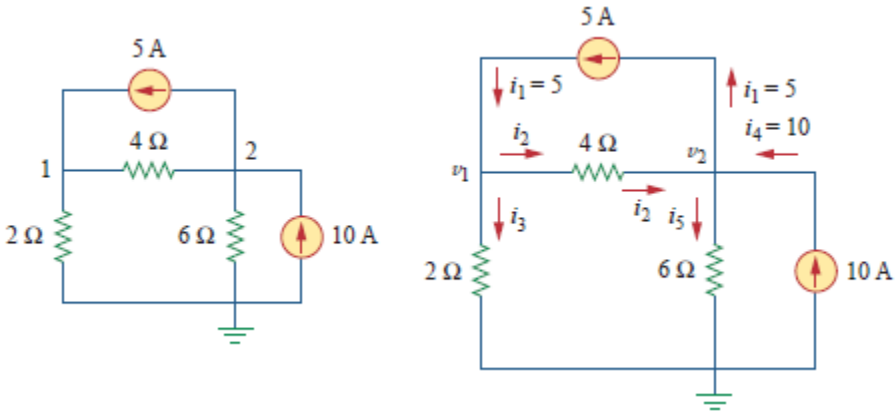


Fig. 2.7: Typical circuit for nodal analysis.

Example 2.4: Find v_1 and v_2 using nodal analysis:



Answer: At node 1, applying KCL and Ohm's law gives

node 1: $$i_1 = i_2 + i_3$$

$$5 = \frac{v_1 - v_2}{4} + \frac{v_1 - 0}{2} \quad (1)$$

node 2: $$i_2 + i_4 = i_1 + i_5$$

$$\frac{v_1 - v_2}{4} + 10 = 5 + \frac{v_2 - 0}{6} \quad (2)$$

from (1) and (2) $v_1 = 13.33V \quad and \; v_2 = 20V.$

Nodal analysis with voltage source is called super-node (A super-node is formed by enclosing a (dependent or independent) voltage source connected between two non-reference nodes and any elements connected in parallel with it.) and considers as special case.

- **CASE 1** If a voltage source is connected between the reference node and a non-reference node, we simply set the voltage at the non-reference node equal to the voltage of the voltage source. In figure 2.8., for example,

$$v_1 = 10V$$

Thus, our analysis is somewhat simplified by this knowledge of the voltage at this node.

- **CASE 2** If the voltage source (dependent or independent) is connected between two non-reference nodes, the two non-reference nodes form a generalized node or super-node; we apply both KCL and KVL to determine the node voltages. We can solve the following three equation to find all three voltages.

$$i_1 + i_4 = i_2 + i_3$$

$$\frac{v_1 - v_2}{2} + \frac{v_1 - v_3}{4} = \frac{v_2 - 0}{8} + \frac{v_3 - 0}{6} \; (1)$$

$$v_2 - v_3 = 5 \; (2) \qquad v_1 = 10 \; (3)$$

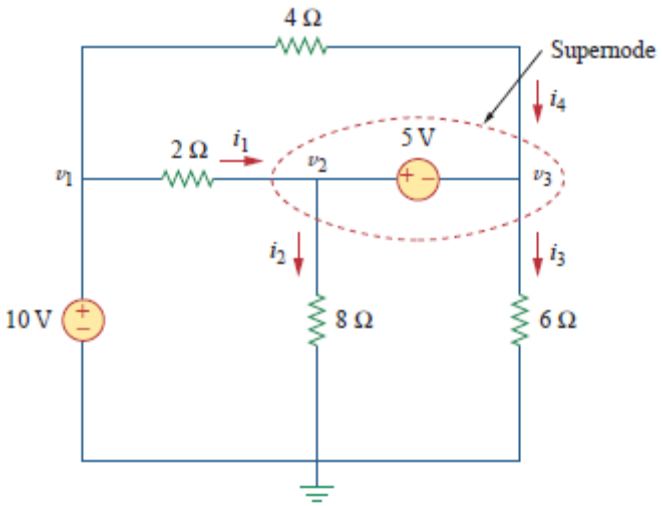


Fig. 2.8: Nodal analysis with voltage source

2.5 Mesh analysis

In the mesh analysis of a circuit with n meshes, we take the following three steps.

- Assign mesh currents $i_1, i_2, \ldots, i_n$ to the n meshes.
- Apply KVL to each of the n meshes. Use Ohm's law to express the voltages in terms of the mesh currents.
- Solve the resulting n simultaneous equations to get the mesh currents.

As shown in figure 2.9,
loop 1:

$$-V_1 + R_1 i_1 + R_3(i_1 - i_2) = 0$$

loop 2:

$$R_2 i_2 + V_2 + R_3(i_2 - i_1) = 0$$

After we will solve the two equation we can find:

$$I_1 = i_1, \quad I_2 = i_2 \; and \; I_3 = i_1 - i_2$$

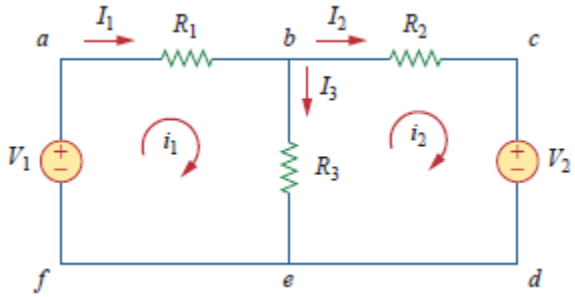
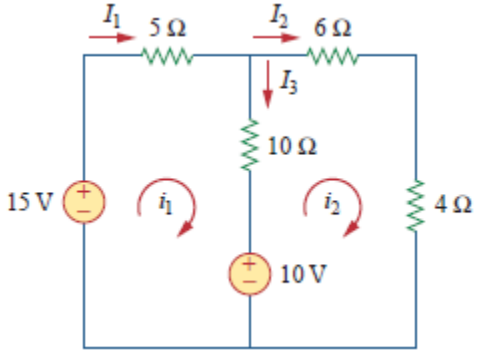


Fig. 2.9: Typical circuit for mesh analysis.

Example 2.5: Find the branch currents I_1, I_2 and I_3 using mesh analysis.



Answer: We first obtain the mesh currents using KVL. For mesh 1,

$$-15 + 5i_1 + 10(i_1 - i_2) + 10 = 0 \; (1)$$

and for mesh 2

$$6i_2 + 4i_2 + 10(i_2 - i_1) - 10 = 0 \; (2)$$

from (1) and (2)

$$i_1 = i_2 = 1A$$

$$I_1 = i_1 = 1A, \quad I_2 = i_2 = 1A \; and \; I_3 = i_1 - i_2 = 0A$$

Mesh Analysis with Current Sources is called super-mesh (A super-mesh results when two meshes have a (dependent or independent) current source in common..) and considers as special case.

- **CASE 1** When a current source exists only in one mesh: Consider the circuit in figure 2.10(c), for example. We set $i_2 = -5$ A and write a mesh equation for the other mesh in the usual way; that is,

$$v_1 = 10V$$

Thus, our analysis is somewhat simplified by this knowledge of the voltage at this node.

- **CASE 2** When a current source exists between two meshes: Consider the circuit in figure 2.10(a), for example. We create a super-mesh by excluding the current source and any elements connected in series with it, as shown in figure 2.10(b).

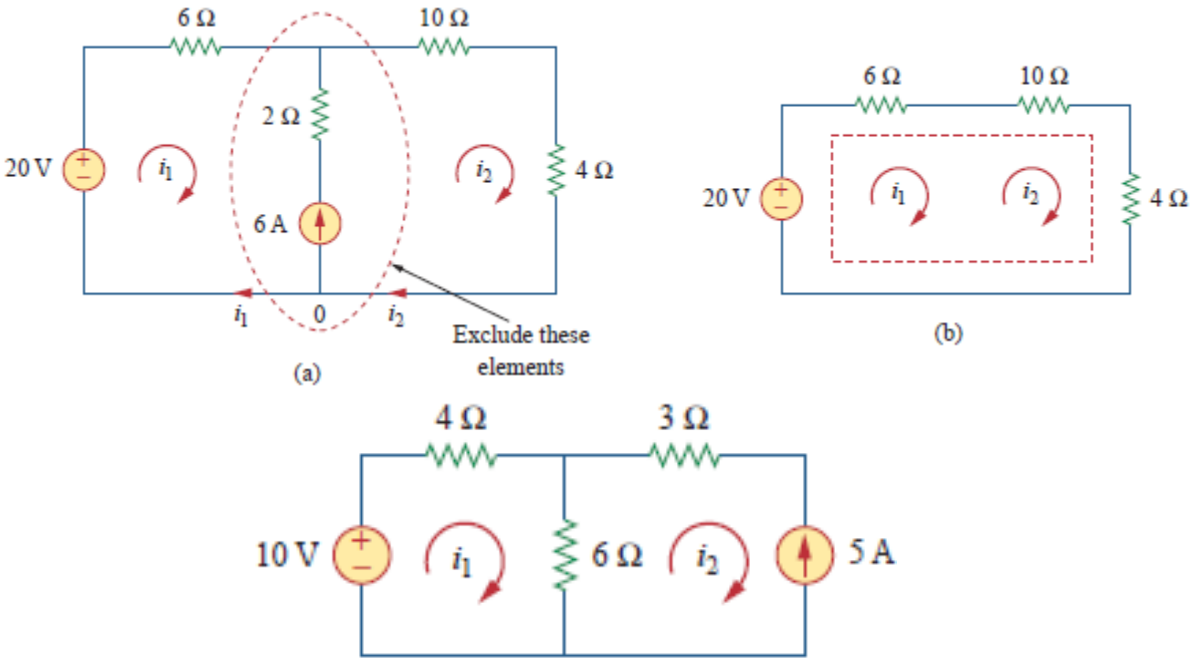


Fig. 2.10: Mesh analysis with current source

2.6 Superposition

The superposition principle states that the voltage across (or current through) an element in a linear circuit is the algebraic sum of the voltages across (or currents through) that element due to each independent source acting alone. With these in mind, we apply the superposition principle in three steps:

- Turn off all independent sources except one source. Find the output (voltage or current) due to that active source using the techniques covered in this chapter.
- Repeat step 1 for each of the other independent sources.
- Find the total contribution by adding algebraically all the contributions due to the independent sources.

Example 2.6: Use the superposition theorem to find v in the circuit of figure 2.11.

Answer:

$$v = v_1 + v_2$$

from figure 2.11a by voltage divider

$$v_1 = 4i_1 = \frac{4}{4+8} * 6 = 2V$$

from figure 2.11b by current divider

$$v_2 = 4i_3 = 4 * \frac{8}{4+8} * 3 = 8V$$

$$v = v_1 + v_2 = 2 + 8 = 10V$$

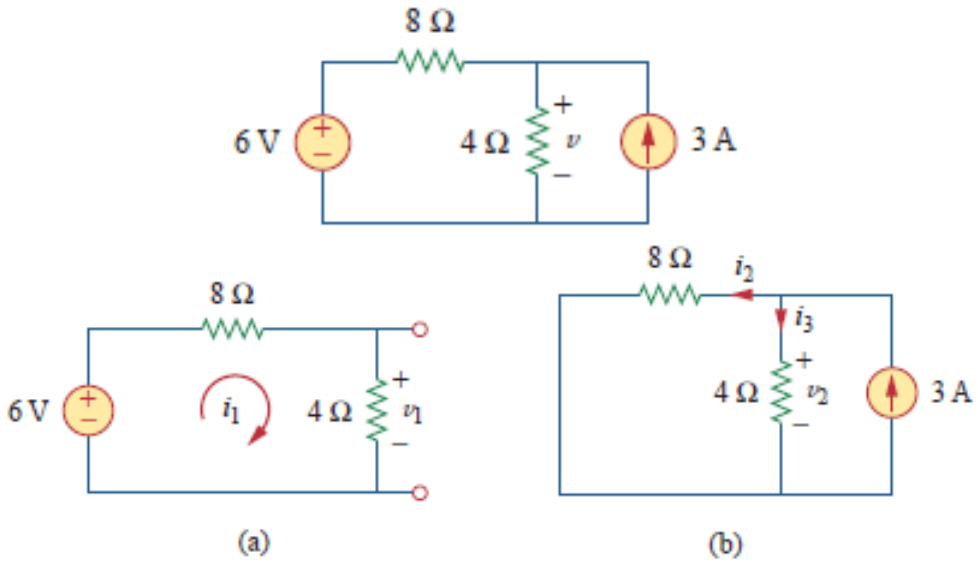


Fig. 2.11: Superposition circuits

2.7 Thevenin's theorem

Thevenin's theorem states that a linear two-terminal circuit can be replaced by an equivalent circuit consisting of a voltage source V_{Th} in series with a resistor R_{Th}, where V_{Th} is the open-circuit voltage at the terminals and R_{Th} is the input or equivalent resistance at the terminals when the independent sources are turned off as shown in figure 2.12.

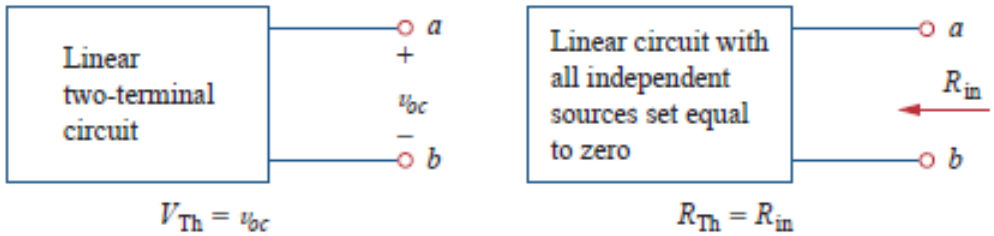
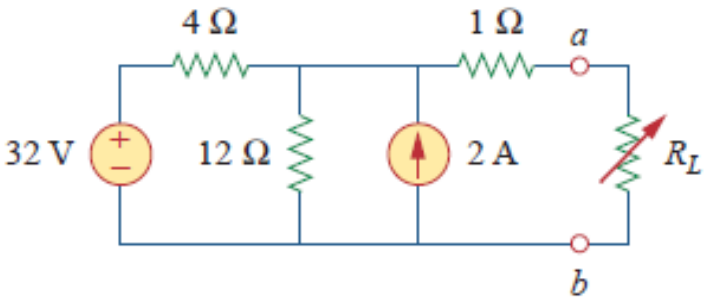


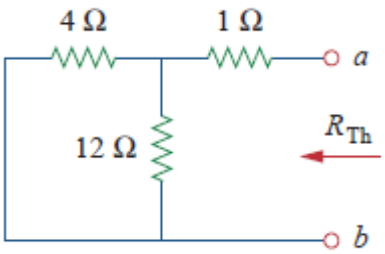
Fig. 2.12: Thevenin's circuits

Example 2.7: Find the Thevenin equivalent circuit of the circuit shown, to the left of the terminals a - b.



Answer:

R_{th}= (4//12)+1= 4Ω

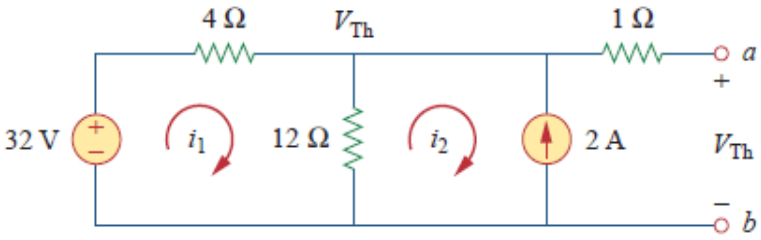


$$i_2 = -2A$$

$$-32 + 16i_1 - 12i_2 = 0$$

$$i_1 = 0.5A$$

$$V_{Th} = 12(i_1 - i_2) = 30V$$



2.8 Norton theorem

Norton's theorem states that a linear two-terminal circuit can be replaced by an equivalent circuit consisting of a current source $I_N = V_{Th}/R_{Th}$ in parallel with a resistor $R_N = R_{Th}$, where I_N is the short-circuit current through the terminals and R_N is the input or equivalent resistance at the terminals when the independent sources are turned off.

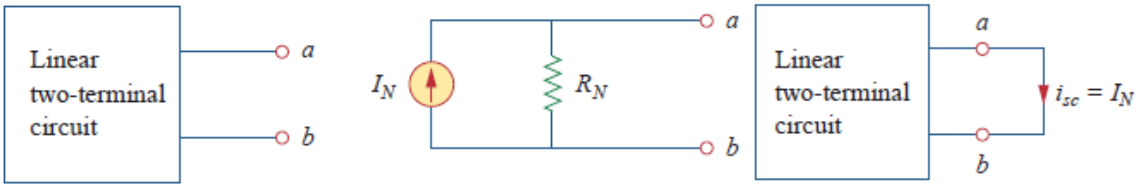
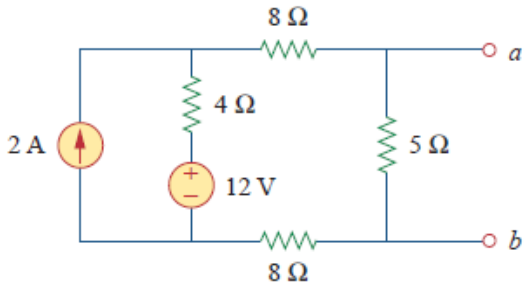


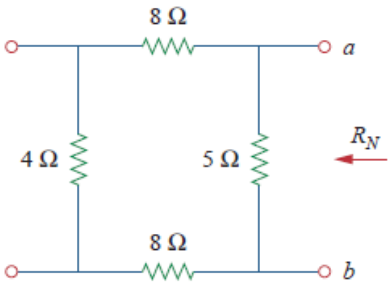
Fig. 2.13: Norton circuits

Example 2.8: Find the Norton equivalent circuit of the circuit shown, to the left of the terminals a - b.



Answer:

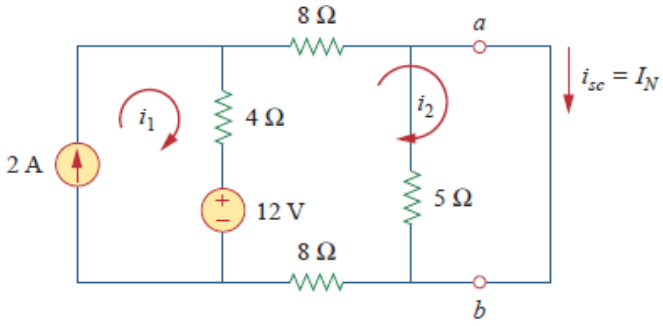
R_N =5//(8+4+8)=4Ω



$$i_1 = 2A$$

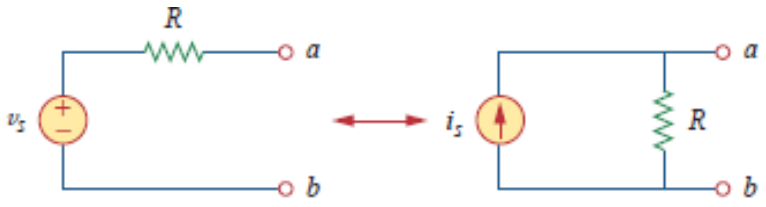
$$20i_2 - 4i_1 - 12 = 0$$

$$i_2 = 1A = i_{sc} = I_N$$



2.9 Source transformation

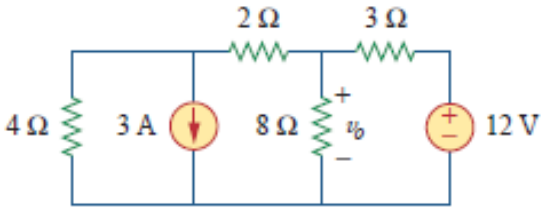
A source transformation is the process of replacing a voltage source v_s in series with a resistor R by a current source is in parallel with a resistor R, or vice versa as shown in figure 2.14.



$$v_s = i_s R \quad \text{or} \quad i_s = \frac{v_s}{R}$$

Fig. 2.14: Source transformation circuits

Example 2.9: Use source transformation to find v_0 in the following circuit.



Answer: We first transform the current and voltage sources to obtain the circuit in figure 2.15(a). Combining the 4Ω and 2Ω resistors in series and transforming the 12-V voltage source gives us figure 2.15(b). We now combine the 3Ω and 6Ω resistors in parallel to get 2Ω . We also combine the 2-A and 4-A current sources to get a 2-A source. Thus, by repeatedly applying source transformations, we obtain the circuit in figure 2.15(c).

$$v_0 = 8i = 8 * \frac{2}{2+8} * 2 = 3.2V$$

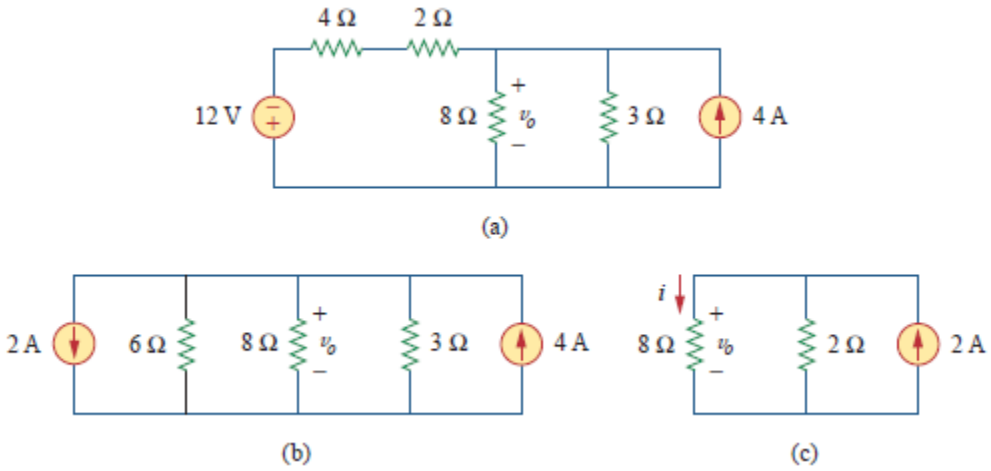
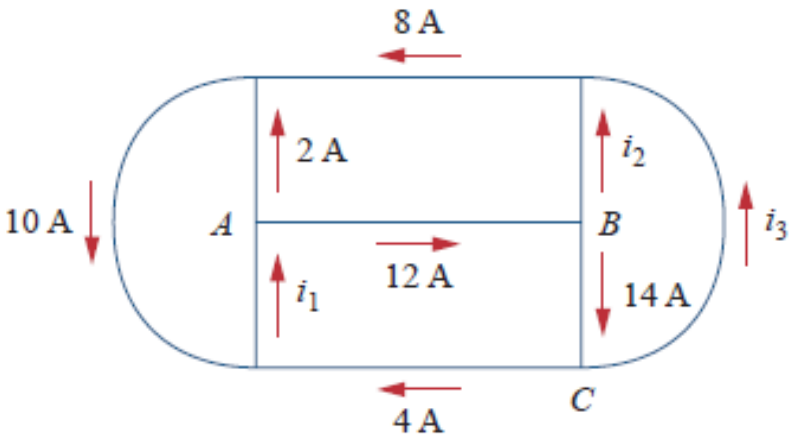


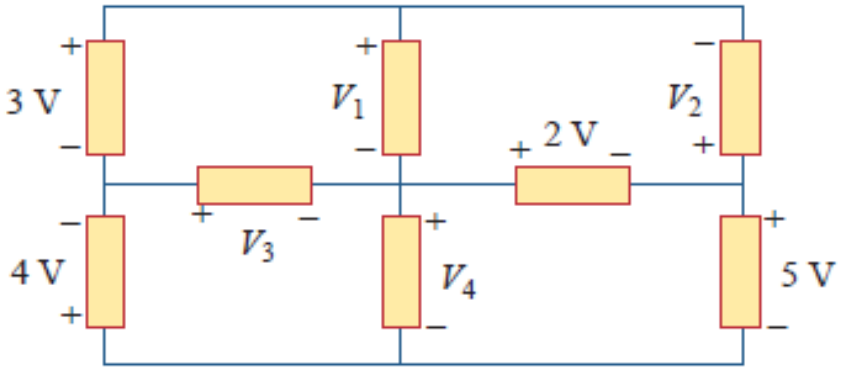
Fig. 2.15: Source transformation example

2.10 Sheet 2

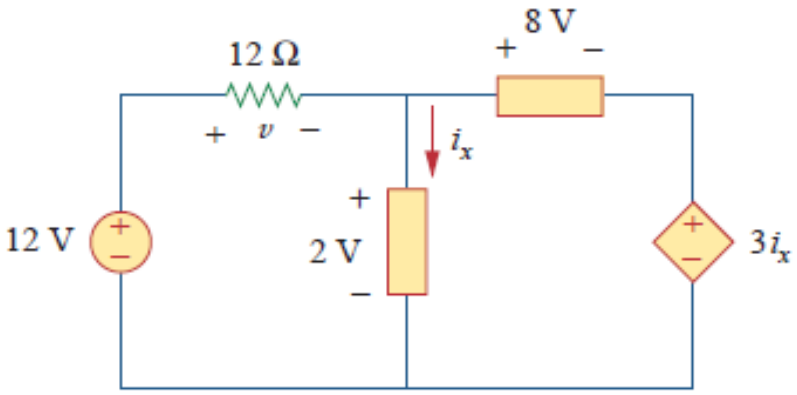
1. Find i_1, i_2, and i_3 in the following figure:



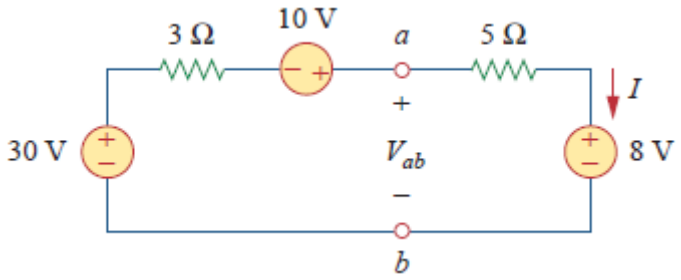
2. Given the circuit in the following figure, use KVL to find the branch voltages V_1 to V_4.



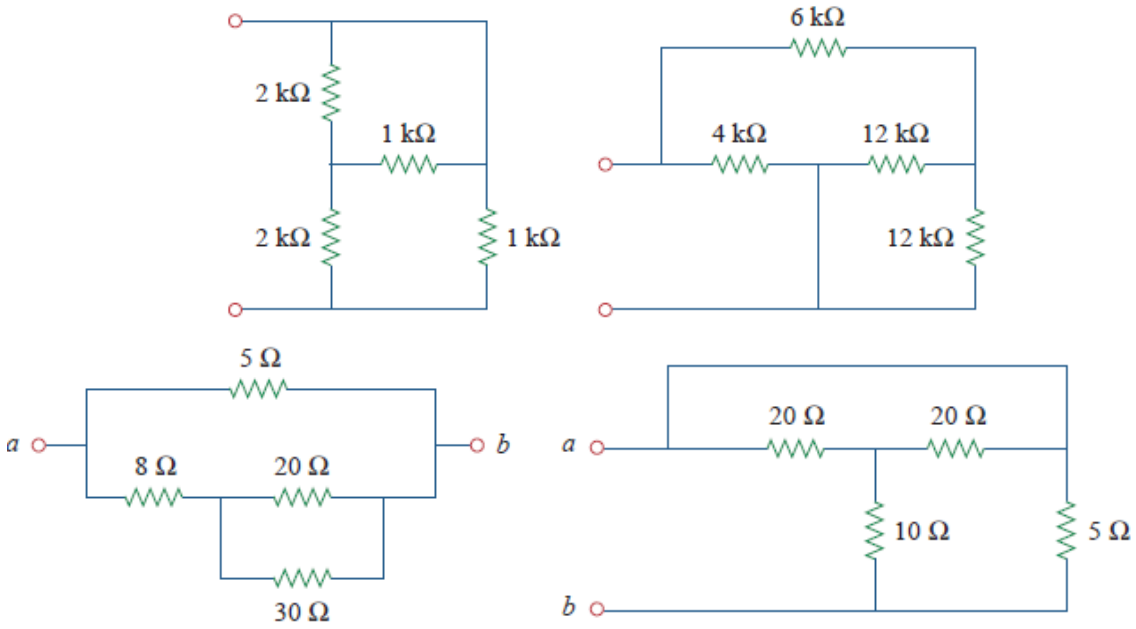
3. Calculate v and i_x in the circuit of the following figure:



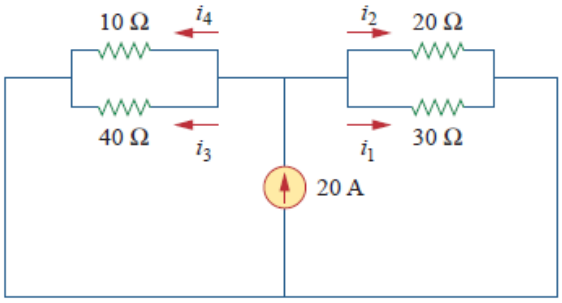
4. Find I and V_{ab} in the circuit of the following figure:



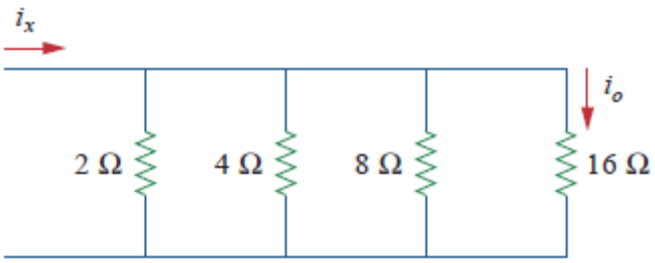
5. Evaluate R_{eq} for each of the circuits shown in the following figure:



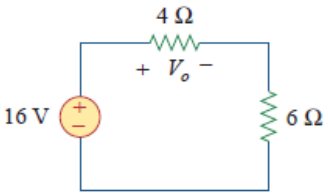
6. Find i_1 through i_4 in the circuit of the following circuit:



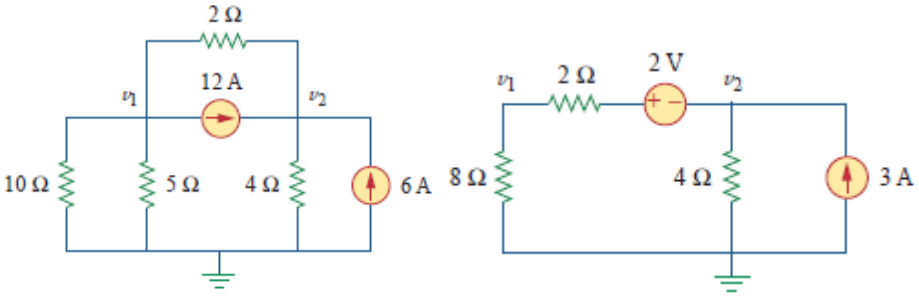
7. For the circuit in the following figure, i_0= 2A. Calculate i_x and the total power dissipated by the circuit.



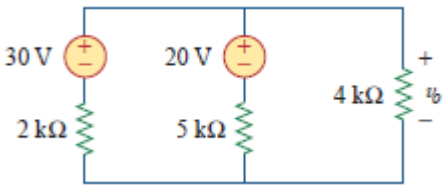
8. Calculate V_o in the circuit of the following figure:



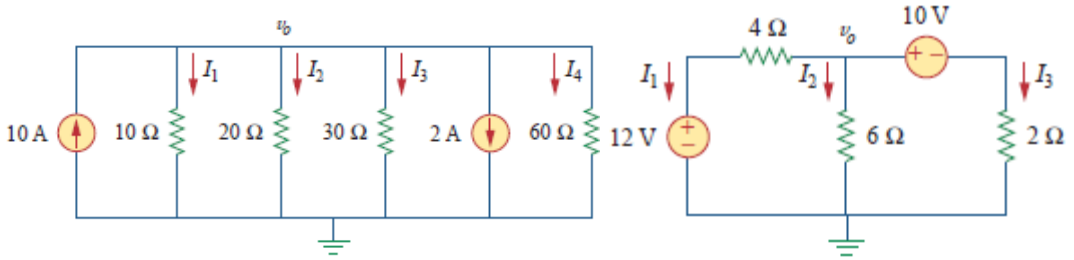
9. For the circuit in the following figures, obtain v_1 and v_2 by using nodal analysis.



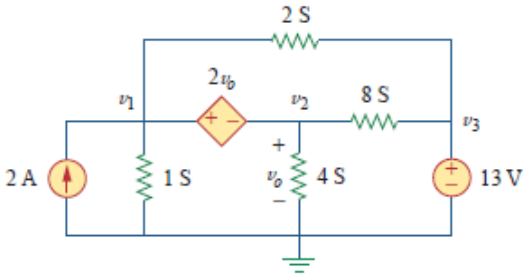
10. For the circuit in the following figures, obtain v_0 by using nodal analysis.



(a)

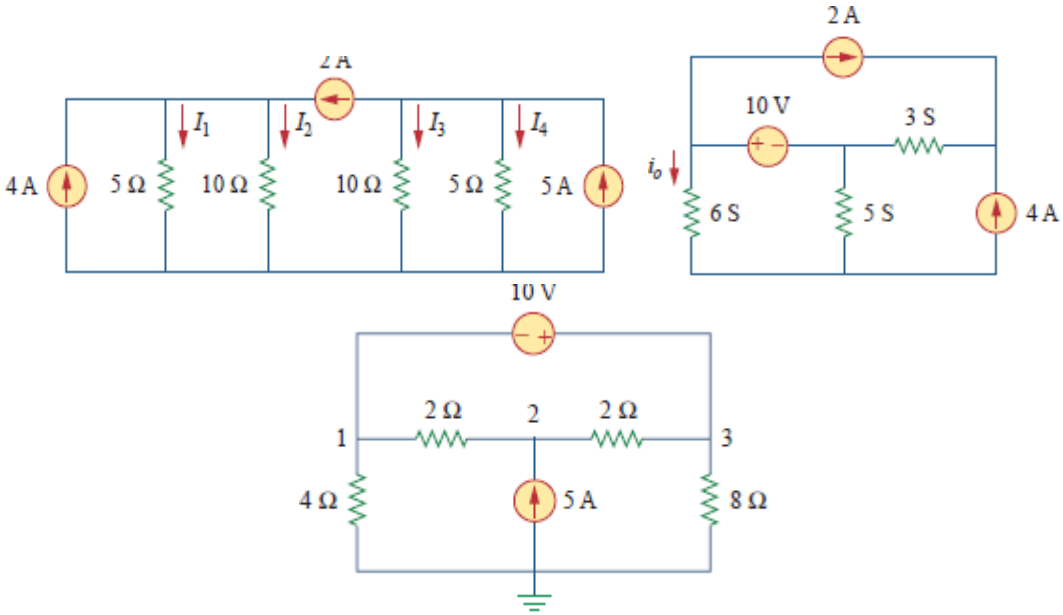


(b) (c)



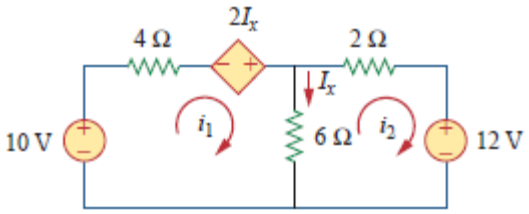
(d)

11. For the circuit in the following figures, find all node voltages by using nodal analysis.

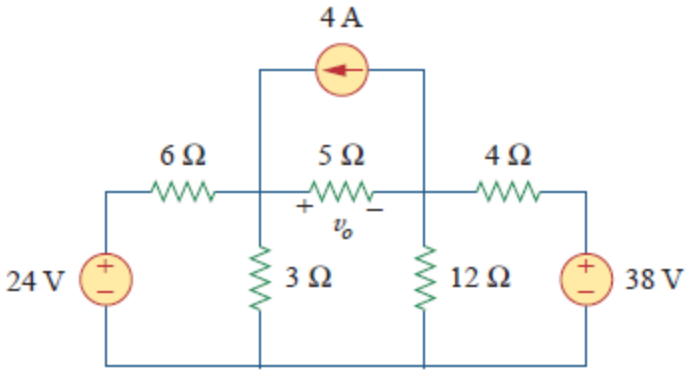


12. Repeat all the previous problems by using mesh analysis

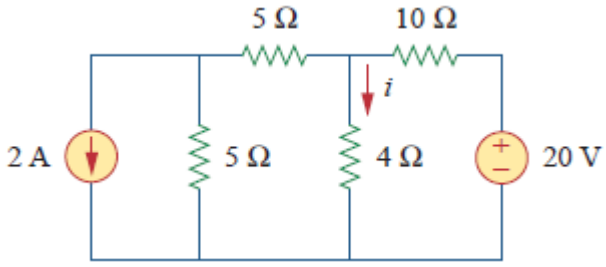
13. For the circuit in the following figures, find all currents



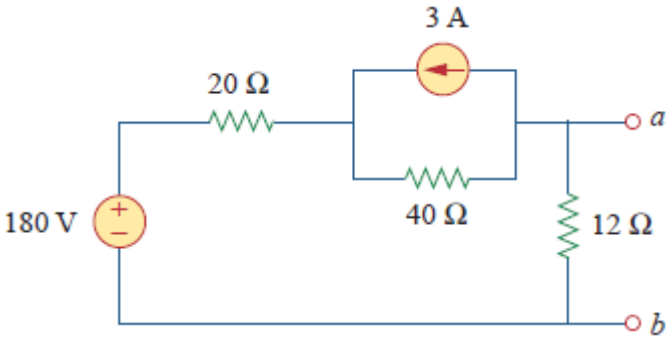
14. Determine v_0 in the circuit using the superposition principle.



15. For the circuit, use source transformation to find *i*.



16. Find the Norton and Thevenin's equivalent with respect to terminals a-b in the circuit shown



CHAPTER 3

NATURAL AND STEP RESPONSE FOR RL, RC AND RLC CIRCUIT

CHAPTER 3

NATURAL AND STEP RESPONSE FOR RL, RC AND RLC CIRCUIT

3.1 Inductors

An inductor is a passive element designed to store energy in its magnetic field. Inductors find numerous applications in electronic and power systems. They are used in power supplies, transformers, radios, TVs, radars, and electric motors. Any conductor of electric current has inductive properties and may be regarded as an inductor. But in order to enhance the inductive effect, a practical inductor is usually formed into a cylindrical coil with many turns of conducting wire, as shown in as shown in figure 3.1. An inductor consists of a coil of conducting wire.

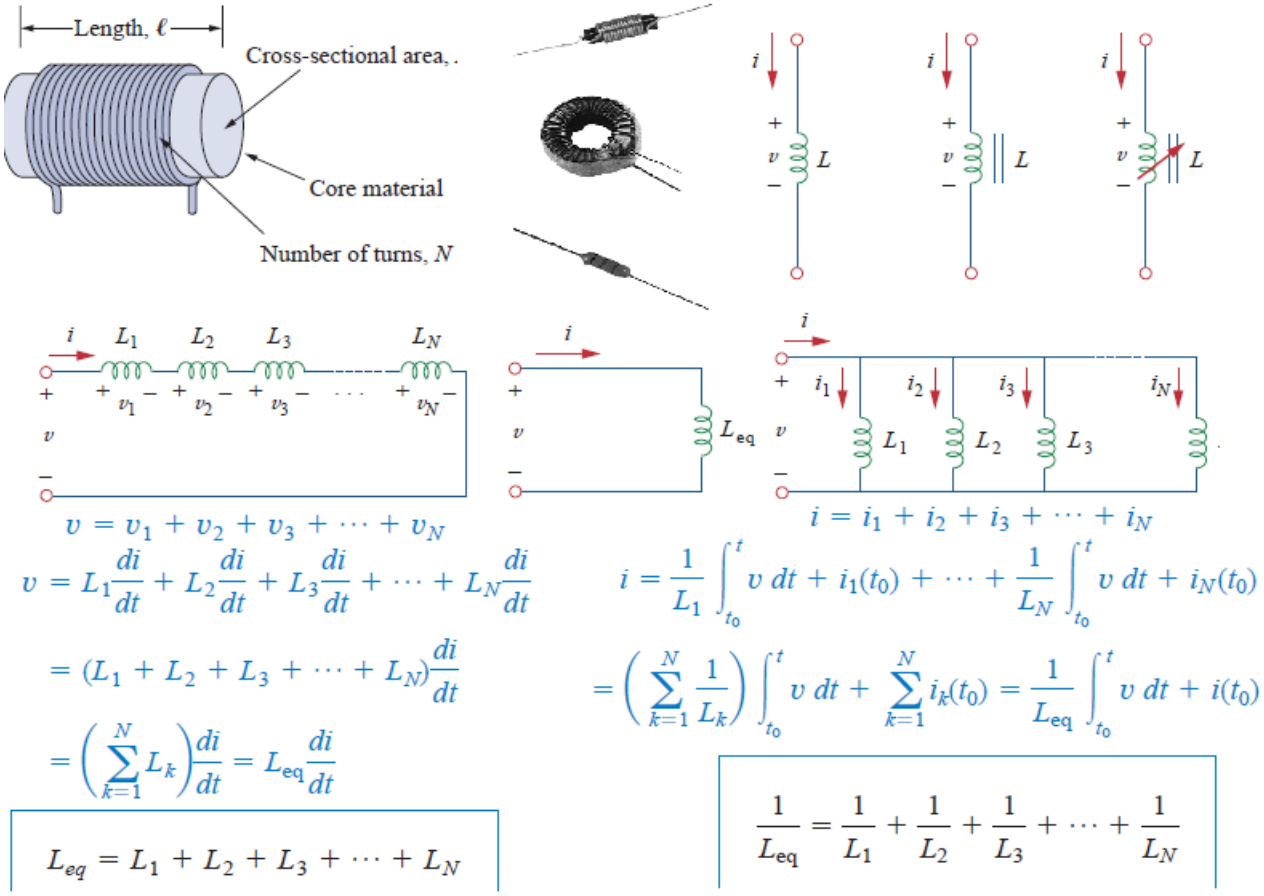


Fig. 3.1: Inductors

Inductance is the property whereby an inductor exhibits opposition to the change of current flowing through it, measured in henrys (H).

$$L = N^2 \mu A/l$$

where N is the number of turns, l is the length, A is the cross-sectional area, and μ is the permeability of the core

3.2 Capacitors

A capacitor is a passive element designed to store energy in its electric field. Besides resistors, capacitors are the most common electrical components. Capacitors are used extensively in electronics, communications, computers, and power systems.

1F= 1C/1V

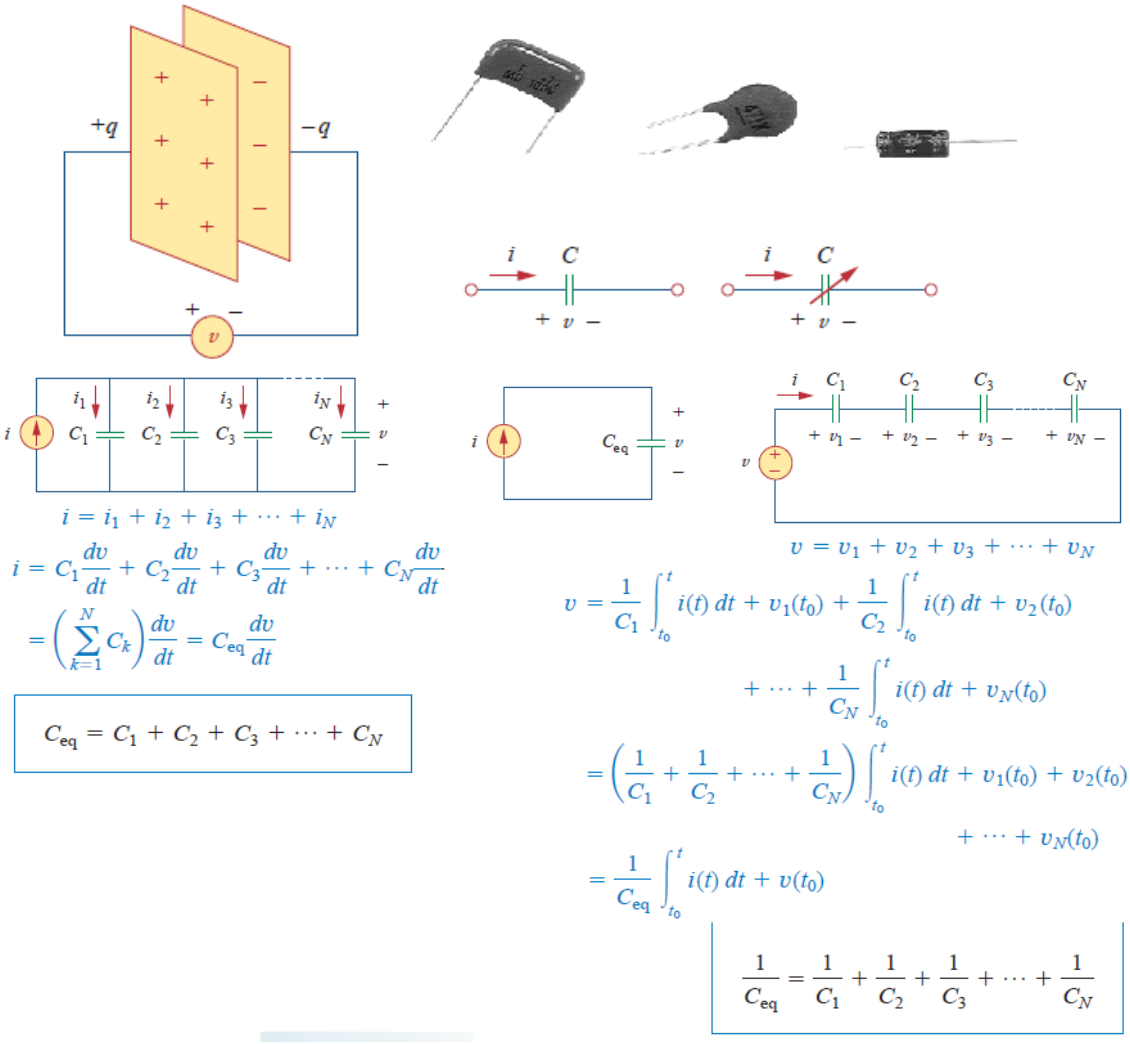


Fig. 3.2: Capacitors

For example, they are used in the tuning circuits of radio receivers and as dynamic memory elements in computer systems. A capacitor consists of two conducting plates separated by an insulator (or dielectric) as shown in figure 3.2.

$$q=CV \text{ and } C=\text{Ɛ}A/d$$

where A is the surface area of each plate, d is the distance between the plates, and Ɛ is the permittivity of the dielectric material between the plates. Capacitance is the ratio of the charge on one plate of a capacitor to the voltage difference between the two plates, measured in farads (F). As shown in figure 3.3, we can present a complete comparison between the three passive element.

Important characteristics of the basic elements.†

Relation	Resistor (R)	Capacitor (C)	Inductor (L)
v-i:	$v = iR$	$v = \frac{1}{C}\int_{t_0}^{t} i\,dt + v(t_0)$	$v = L\frac{di}{dt}$
i-v:	$i = v/R$	$i = C\frac{dv}{dt}$	$i = \frac{1}{L}\int_{t_0}^{t} v\,dt + i(t_0)$
p or w:	$p = i^2R = \frac{v^2}{R}$	$w = \frac{1}{2}Cv^2$	$w = \frac{1}{2}Li^2$
Series:	$R_{eq} = R_1 + R_2$	$C_{eq} = \frac{C_1C_2}{C_1 + C_2}$	$L_{eq} = L_1 + L_2$
Parallel:	$R_{eq} = \frac{R_1R_2}{R_1 + R_2}$	$C_{eq} = C_1 + C_2$	$L_{eq} = \frac{L_1L_2}{L_1 + L_2}$
At dc:	Same	Open circuit	Short circuit
Circuit variable that cannot change abruptly:	Not applicable	v	i

Fig. 3.3: Comparison between capacitors, inductors and resistors.

3.3 First order transient circuit

In this chapter, we shall examine two types of simple circuits: a circuit comprising a resistor and capacitor and a circuit comprising a resistor and an inductor. These are called RC and RL circuits, respectively. A first-order circuit is characterized by a first-order differential equation. The meaning of transient is shown in figure 3.4.

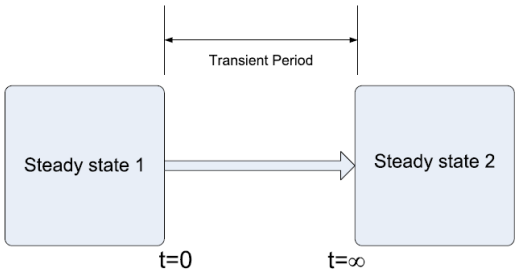


Fig. 3.4: Meaning of transient

3.3.1 Source free R-C circuit

A source-free *RC* circuit occurs when its dc source is suddenly disconnected. The energy already stored in the capacitor is released to the resistors (sometimes called free response) as shown in figure 3.5. This shows that the voltage response of the RC circuit is an exponential decay of the initial voltage. Since the response is due to the initial energy stored and the physical characteristics of the circuit and not due to some external voltage or current source, it is called the natural response of the circuit.

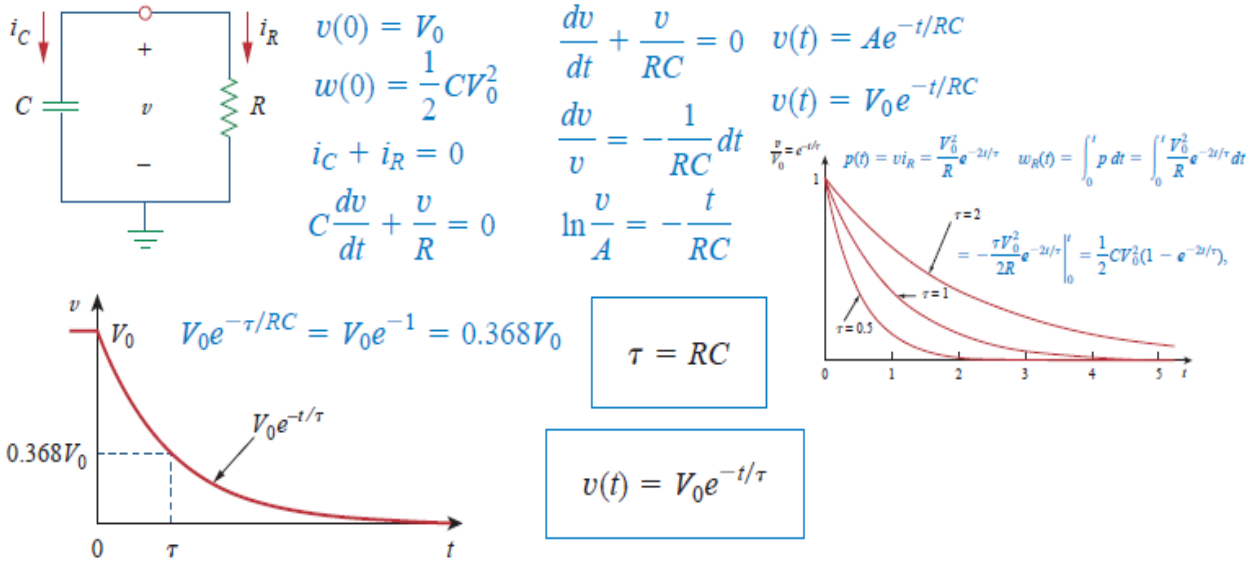
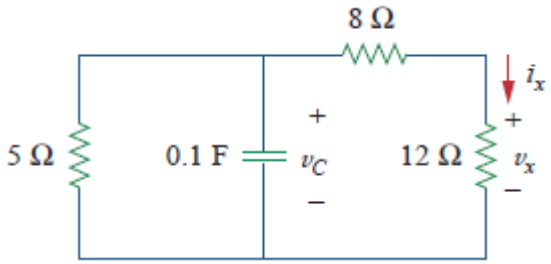


Fig. 3.5: Source free R-C circuit

The time constant of a circuit is the time required for the response to decay to a factor of 1/e or 36.8 percent of its initial value. The Key to Working with a Source-free RC Circuit Is Finding:

- The initial voltage v(0) = V_0 across the capacitor.
- The time constant τ.

Example 3.3: let Vc(0)=15, find V_c, V_x and i_x for t >0.



Answer: We first need to make the circuit conform with the standard RC circuit.

$$R_{eq} = \frac{20 \times 5}{20 + 5} = 4\ \Omega$$

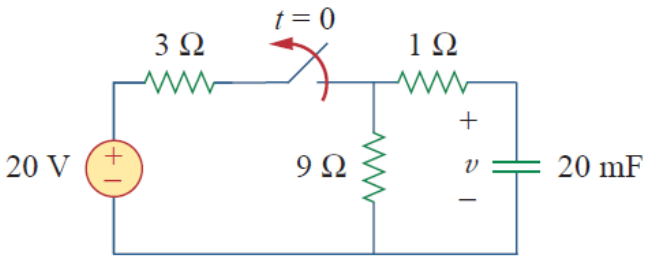
$$\tau = R_{eq}C = 4(0.1) = 0.4\ \text{s}$$

$$v = v(0)e^{-t/\tau} = 15e^{-t/0.4}\ \text{V}, \qquad v_C = v = 15e^{-2.5t}\ \text{V}$$

$$v_x = \frac{12}{12 + 8}v = 0.6(15e^{-2.5t}) = 9e^{-2.5t}\ \text{V}$$

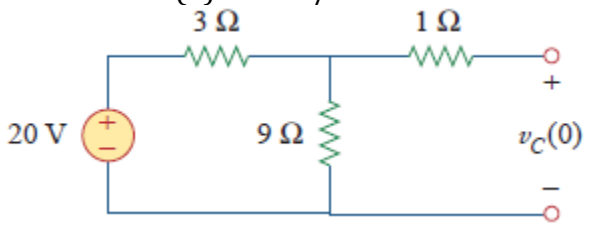
$$i_x = \frac{v_x}{12} = 0.75e^{-2.5t}\ \text{A}$$

Example 3.4: the switch in the circuit in the following Fig. has been closed for a long time, and it is opened at t =0. Find v(t) for t ≥ 0. Calculate the initial energy stored in the capacitor.

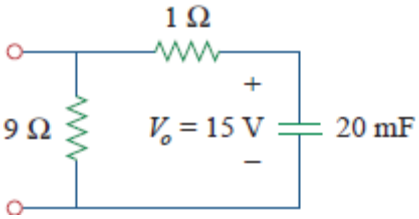


Answer: For t < 0 the switch is closed; the capacitor is an open circuit to dc, as represented in the following figure. Using voltage division

Vc(o) = 20*9/12 =15V



For the switch is opened, and we have the RC circuit shown in the following figure.



[Notice that the RC circuit is source free] The resistors in series give

$$R_{eq} = 9 + 1 = 10$$

The time constant is

$$\tau = R_{eq} * C = 0.2s$$

Thus, the voltage across the capacitor for is

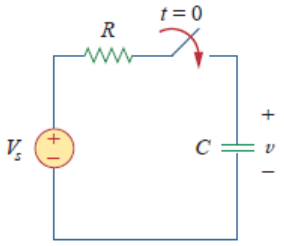
$$v(t) = 15e^{-5t}V$$

The initial energy stored in the capacitor is

$$Wc(0)=0.5\ C*V^2=2.25\ J$$

3.3.2 Forced R-C circuit

The steady-state response is the behavior of the circuit a long time after an external excitation is applied. The forced R-C circuit is shown in figure 3.6. with v(∞) is the final value of capacitor voltage.



$$v(0^-) = v(0^+) = V_0$$

$$C\frac{dv}{dt} + \frac{v - V_s u(t)}{R} = 0$$

$$\frac{dv}{dt} + \frac{v}{RC} = \frac{V_s}{RC}u(t)$$

$$\frac{dv}{dt} = -\frac{v - V_s}{RC}$$

$$\frac{dv}{v - V_s} = -\frac{dt}{RC}$$

$$\ln(v - V_s)\Big|_{V_0}^{v(t)} = -\frac{t}{RC}\Big|_0^t$$

$$\ln(v(t) - V_s) - \ln(V_0 - V_s) = -\frac{t}{RC} + 0$$

$$\ln\frac{v - V_s}{V_0 - V_s} = -\frac{t}{RC}$$

$$\frac{v - V_s}{V_0 - V_s} = e^{-t/\tau}, \qquad \tau = RC$$

$$v - V_s = (V_0 - V_s)e^{-t/\tau}$$

$$v(t) = V_s + (V_0 - V_s)e^{-t/\tau}, \qquad t > 0$$

$$v(t) = \begin{cases} V_0, & t < 0 \\ V_s + (V_0 - V_s)e^{-t/\tau}, & t > 0 \end{cases}$$

$$v(t) = v(\infty) + [v(0) - v(\infty)]e^{-t/\tau}$$

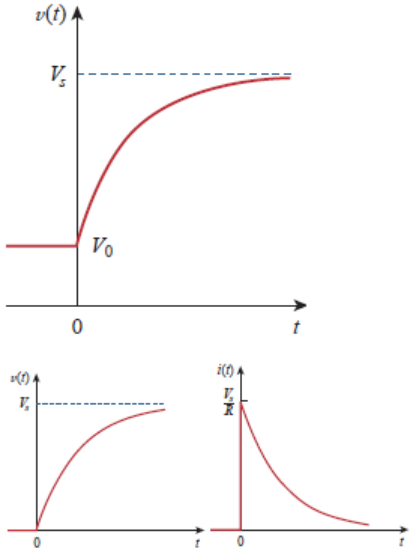
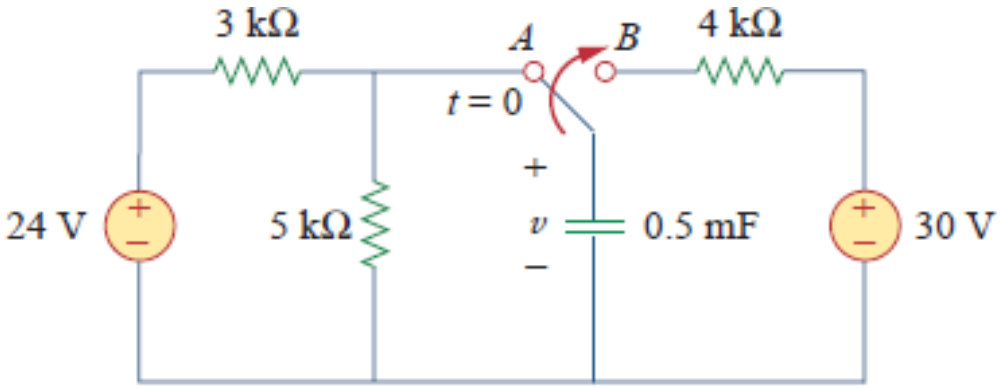


Fig. 3.6: Forced R-C circuit

Example 3.5: the switch in the following Fig. has been in position A for a long time, and it is moved to B at t =0. Determine v(t) for t > 0. Calculate its value at t =1s and t = 4s.



Answer: For t < 0 the switch is at position A. The capacitor acts like an open circuit to dc, but v is the same as the voltage across the resistor 5k. Hence, the voltage across the capacitor just before t=0 is obtained by voltage division as Using the fact that the capacitor voltage cannot change instantaneously,

$$v(0) = \frac{5}{5+3}24 = 15$$

For t>0, the switch is in position B. The Thevenin resistance connected to the capacitor is $R_{Th} = 4\ k$ and the time constant is

$$\tau = R_{eq} * C = 2s$$

Since the capacitor acts like an open circuit to dc at steady state, $v(\infty) = 30$ V

$$v(t) = 30 - 15e^{-0.5t}V$$

at t=1 v=20.9 V

at t=4 v=27.97V

3.3.3 Source free R-L circuit

Consider the series connection of a resistor and an inductor, as shown in Fig. 3.7. Our goal is to determine the circuit response.

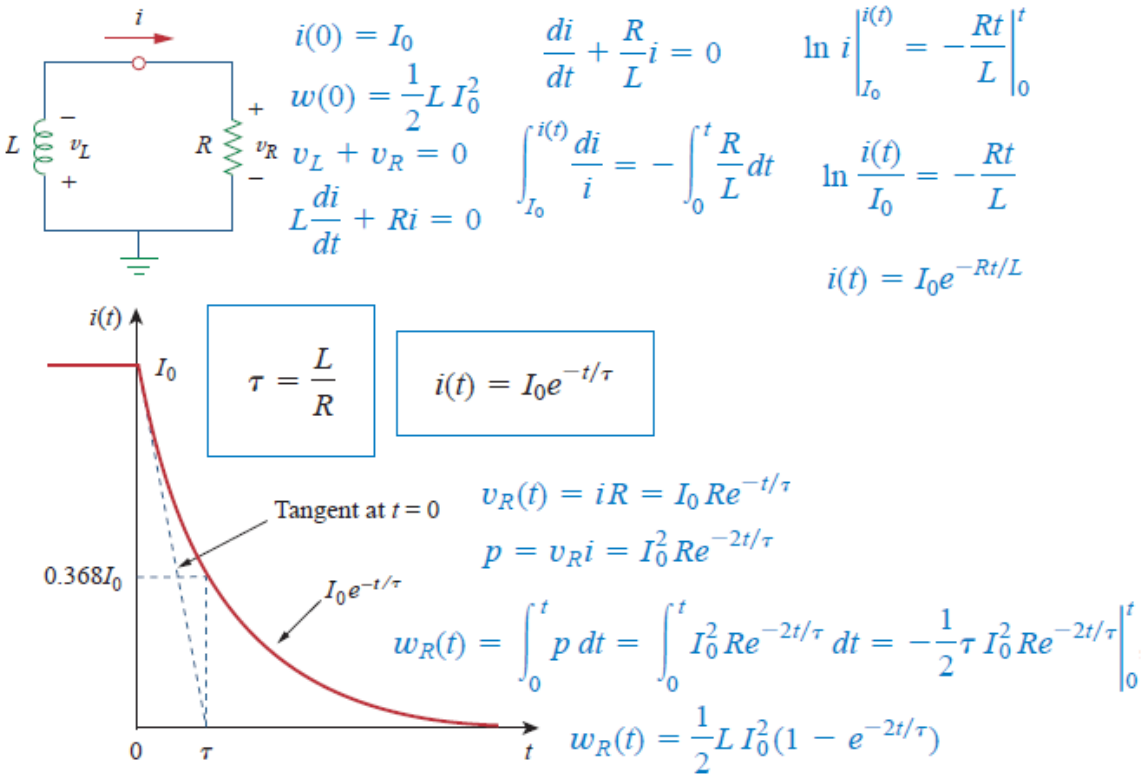
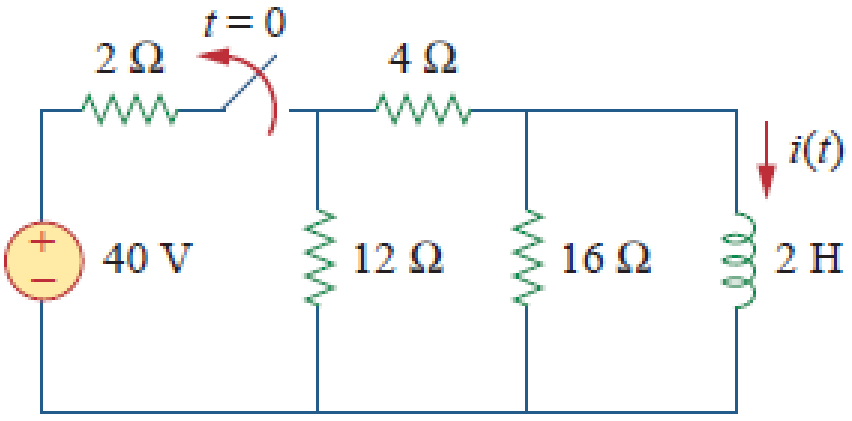


Fig. 3.7: Source free R-L circuit

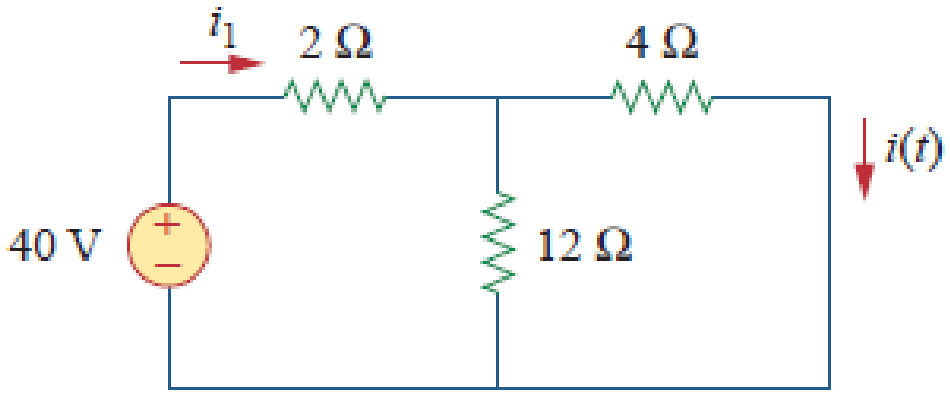
The Key to Working with a Source-free RL Circuit Is Finding:

- The initial current i(0) = I_0 through the inductor.
- The time constant τ.

Example 3.6: the switch in the circuit in the following Fig. has been closed for a long time, and it is opened at t =0. Find i(t) for t ≥ 0



Answer: When t < 0, the switch is closed, and the inductor acts as a short circuit to dc. The resistor 16 is short-circuited; the resulting circuit is shown. To get $i_1$in circuit, we combine the and resistors in parallel.



$$i_1 = \frac{40}{2 + \frac{4 * 12}{12 + 4}} = 8A$$

We obtain i(0) from i_1 using current division, by writing

$$i(t) = \frac{12}{12 + 4} i_1 = 6A$$

When t > 0, the switch is open and the voltage source is disconnected. We now have the source-free RL circuit. Combining the resistors, we have

$$R_{eq} = (12 + 4)//16 = 8\Omega$$

The time constant is

$$\tau = \frac{L}{R_{eq}} = 0.25\ s$$

Thus,

$$i(t) = 6e^{-4t}A$$

3.3.4 Forced R-L circuit

The steady-state response is the behavior of the circuit a long time after an external excitation is applied. The forced R-L circuit is shown in figure 3.8. with i(∞) is the final value of inductor current.

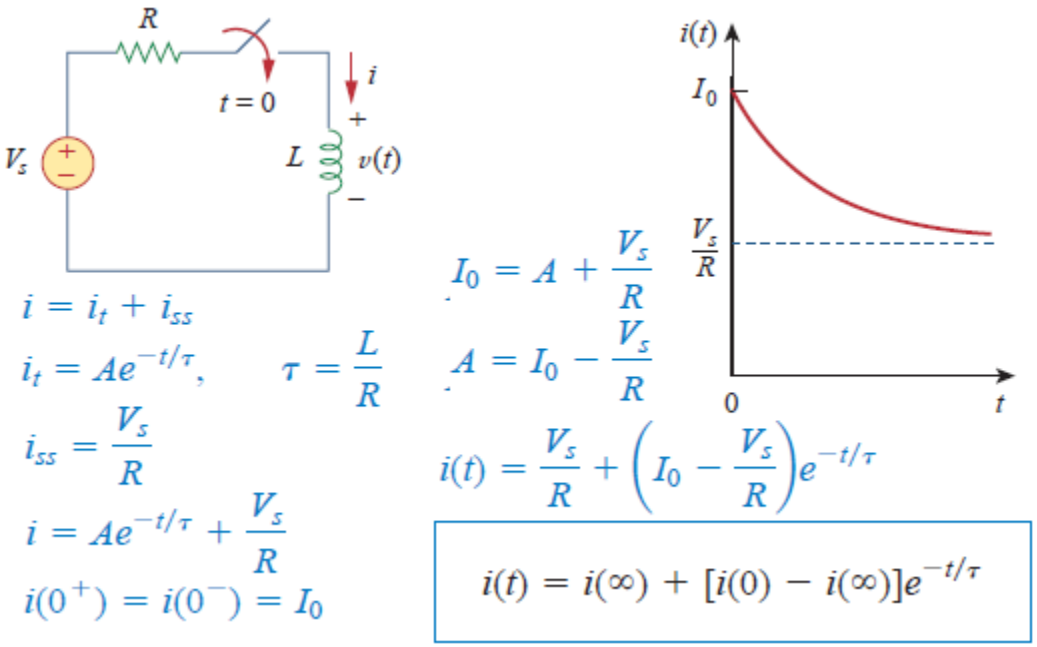
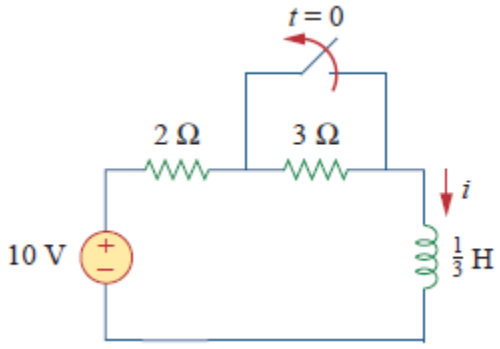


Fig. 3.8: Forced R-L circuit

Example 3.7: Find i(t) in the circuit in the following Fig. for t >0. Assume that the switch has been closed for a long time.



Answer: When t < 0 the 3 ohm resistor is short-circuited, and the inductor acts like a short circuit. The current through the inductor is

$$i(0) = \frac{10}{2} = 5A$$

When t > 0 the switch is open.

$$i(\infty) = \frac{10}{2+3} = 2A$$

The Thevenin resistance across the inductor terminals is

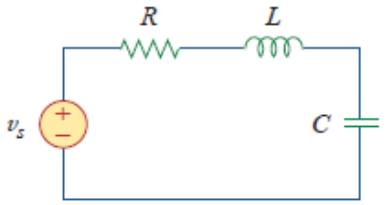
$$R_{Th} = 2 + 3 = 5$$

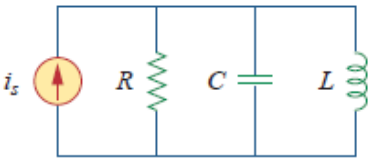
Thus,

$$i(t) = 2 + 3e^{-15t}A$$

3.4 Second order transient circuit

In this chapter we considered circuits with a single storage element (a capacitor or an inductor). Such circuits are first-order because the differential equations describing them are first-order. In this chapter we will consider circuits containing two storage elements. These are known as *second-order* circuits because their responses are described by differential equations that contain second derivatives. Typical examples of second-order circuits are *RLC* circuits, in which the three kinds of passive elements are present. Examples of such circuits are shown in figure 3.9. A second-order circuit is characterized by a second-order differential equation. It consists of resistors and the equivalent of two energy storage elements.





$$i = Ae^{st}$$

$$v(0) = \frac{1}{C}\int_{-\infty}^{0} i\,dt = V_0$$

$$i(0) = I_0$$

$$Ri + L\frac{di}{dt} + \frac{1}{C}\int_{-\infty}^{t} i\,dt = 0$$

$$\frac{d^2i}{dt^2} + \frac{R}{L}\frac{di}{dt} + \frac{i}{LC} = 0$$

$$Ri(0) + L\frac{di(0)}{dt} + V_0 = 0$$

$$\frac{di(0)}{dt} = -\frac{1}{L}(RI_0 + V_0)$$

$$As^2e^{st} + \frac{AR}{L}se^{st} + \frac{A}{LC}e^{st} = 0$$

$$Ae^{st}\left(s^2 + \frac{R}{L}s + \frac{1}{LC}\right) = 0$$

$$\therefore \quad s^2 + \frac{R}{L}s + \frac{1}{LC} = 0$$

$$s_1 = -\frac{R}{2L} + \sqrt{\left(\frac{R}{2L}\right)^2 - \frac{1}{LC}}$$

$$s_2 = -\frac{R}{2L} - \sqrt{\left(\frac{R}{2L}\right)^2 - \frac{1}{LC}}$$

$$s_1 = -\alpha + \sqrt{\alpha^2 - \omega_0^2}, \qquad s_2 = -\alpha - \sqrt{\alpha^2 - \omega_0^2}$$

$$\alpha = \frac{R}{2L}, \qquad \omega_0 = \frac{1}{\sqrt{LC}}$$

Fig. 3.9: source free R-L-C circuit

There are three types of solutions as shown in figure 3.10:

- If $\alpha > w_0$ we have the over-damped case.
- If $\alpha = w_0$ we have the critically damped case.
- If $\alpha < w_0$ we have the under-damped case.

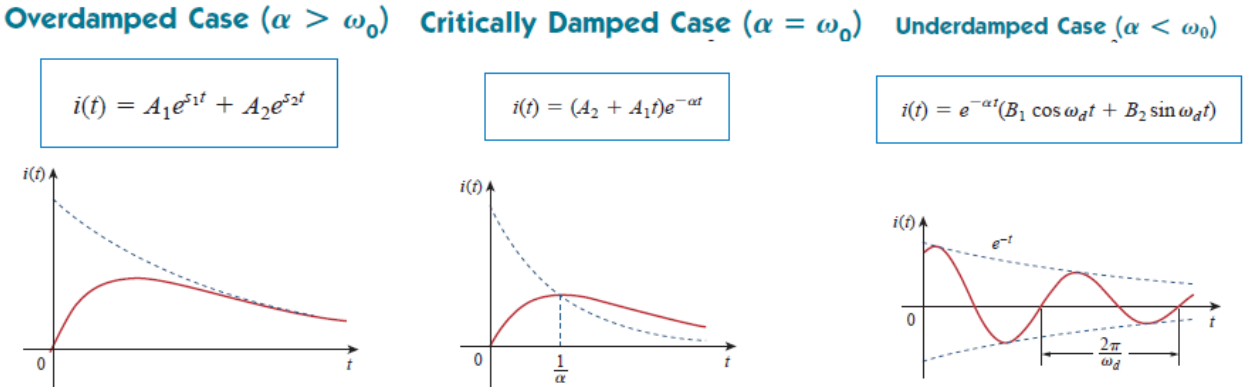
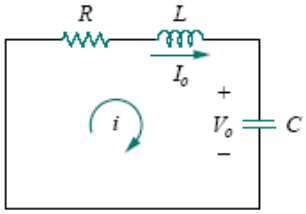


Fig. 3.10: three types of RLC circuit cases.

if we have step response

$$v(t) = V_s + A_1e^{s_1t} + A_2e^{s_2t} \quad \text{(Overdamped)}$$
$$v(t) = V_s + (A_1 + A_2t)e^{-\alpha t} \quad \text{(Critically damped)}$$
$$v(t) = V_s + (A_1 \cos \omega_d t + A_2 \sin \omega_d t)e^{-\alpha t} \quad \text{(Underdamped)}$$

Example 3.8: In the following figure R= 40 ohm, L = 4 H and C= 0.25 F. Calculate the characteristics roots of the circuit. Is the natural response over damped, under damped and critical damped?

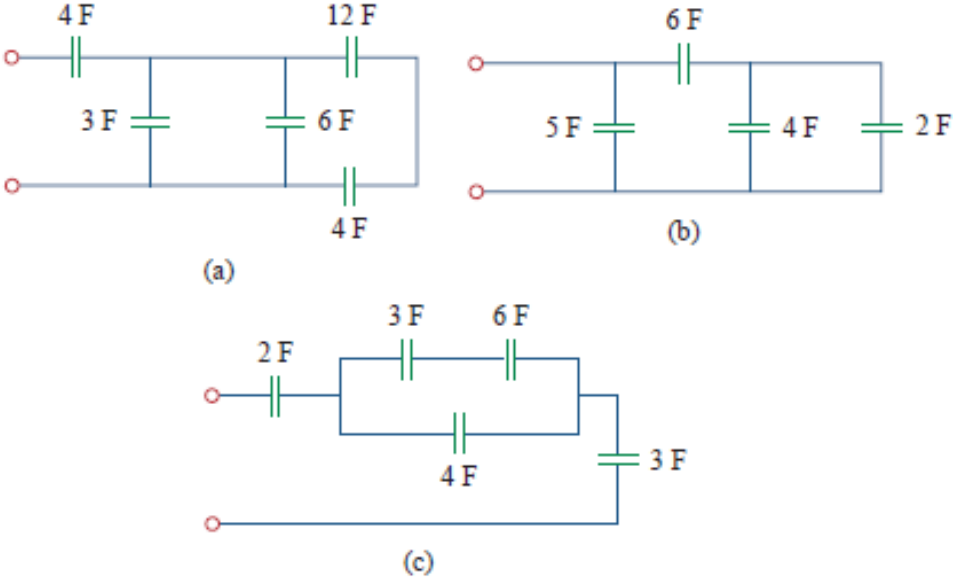


Answer: $\alpha = R/2L = 5$ and $w_0 = \frac{1}{\sqrt{LC}} = 1$

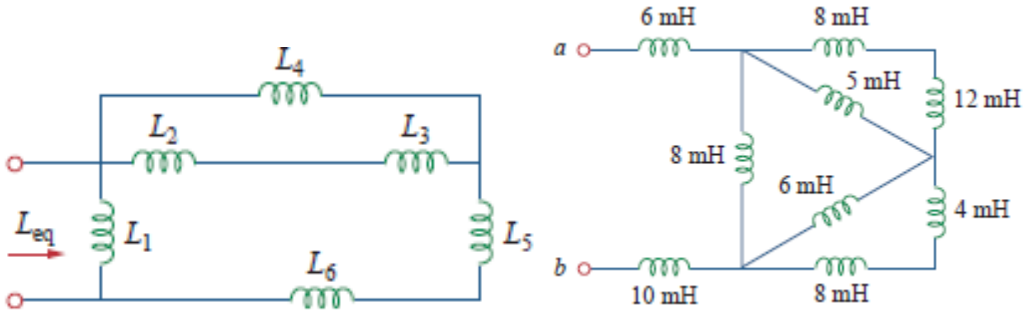
$\alpha > w_0$ the circuit is over-damped $S_1 = -0.101$ and $S_2 = -9.899$

3.5 Sheet 3

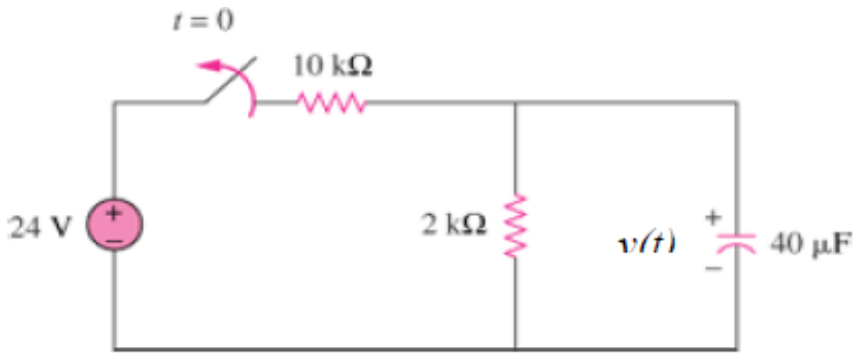
1. Determine the equivalent capacitance for each of the circuits



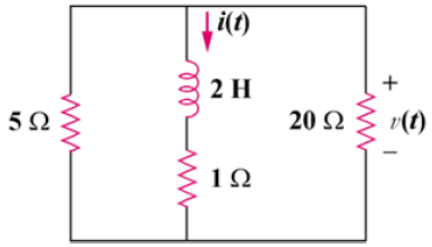
2. Determine the equivalent inductors for each of the circuits



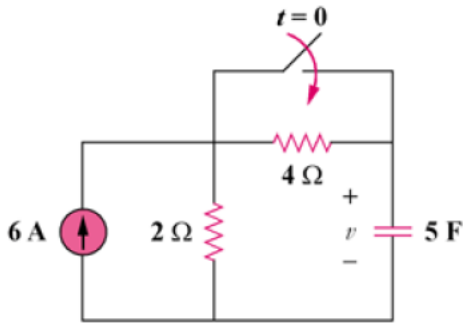
3. The switch in the following figure has been closed for a long time, and it opens at t = 0. Find v(t) for t > 0.



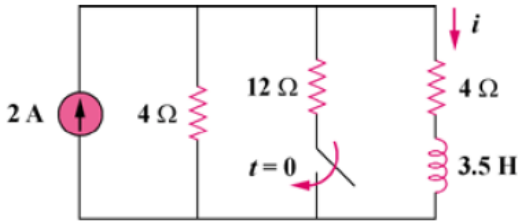
4. Find i(t) and v(t) for t > 0 in the circuit if i(0) = 10 A.



5. Find the capacitor voltage for t < 0 and t > 0 for the circuit

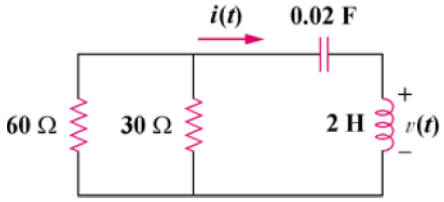


6. Obtain the inductor current for both t < 0 and t > 0 in each of the circuit



7. If R = 20 Ω, L = 0.6 H, what value of C will make an RLC series circuit:
   (a) Over-damped.
   (b) critically damped.
   (c) under-damped.

8. Find v(t) for t > 0 if v(0) = 6 V and i(0) = 2 A in the circuit



CHAPTER 4

SINUSOIDAL STEADY STATE ANALYSIS

CHAPTER 4

SINUSOIDAL STEADY STATE ANALYSIS

4.1 Phasors and sin wave

Thus far our analysis has been limited for the most part to dc circuits: those circuits excited by constant or time-invariant sources. We have restricted the forcing function to dc sources for the sake of simplicity, for pedagogic reasons, and also for historic reasons. Historically, dc sources were the main means of providing electric power up until the late 1800s. At the end of that century, the battle of direct current versus alternating current began. Both had their advocates among the electrical engineers of the time. Because ac is more efficient and economical to transmit over long distances, ac systems ended up the winner. Thus, it is in keeping with the historical sequence of events that we considered dc sources first. We now begin the analysis of circuits in which the source voltage or current is time-varying. In this chapter, we are particularly interested in sinusoidal time-varying excitation, or simply, excitation by a *sinusoid.* A sinusoid is a signal that has the form of the sine or cosine function as shown in figure 4.1.

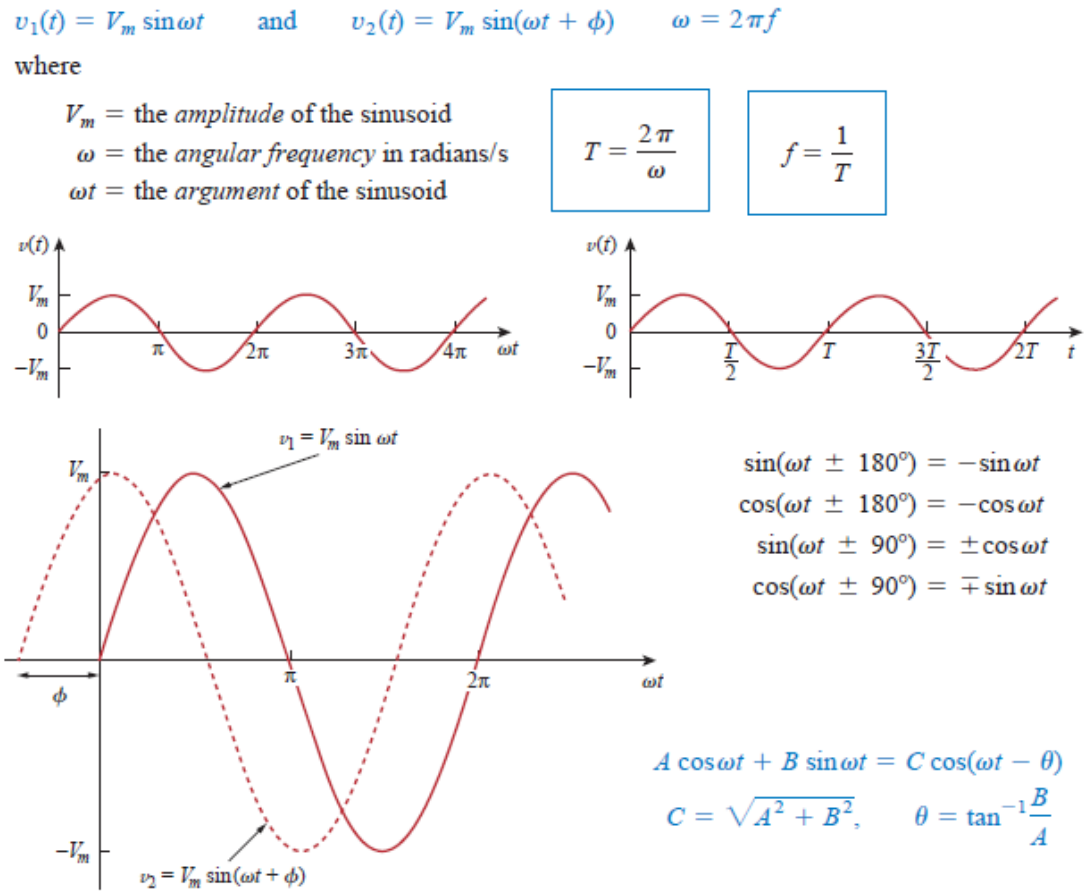
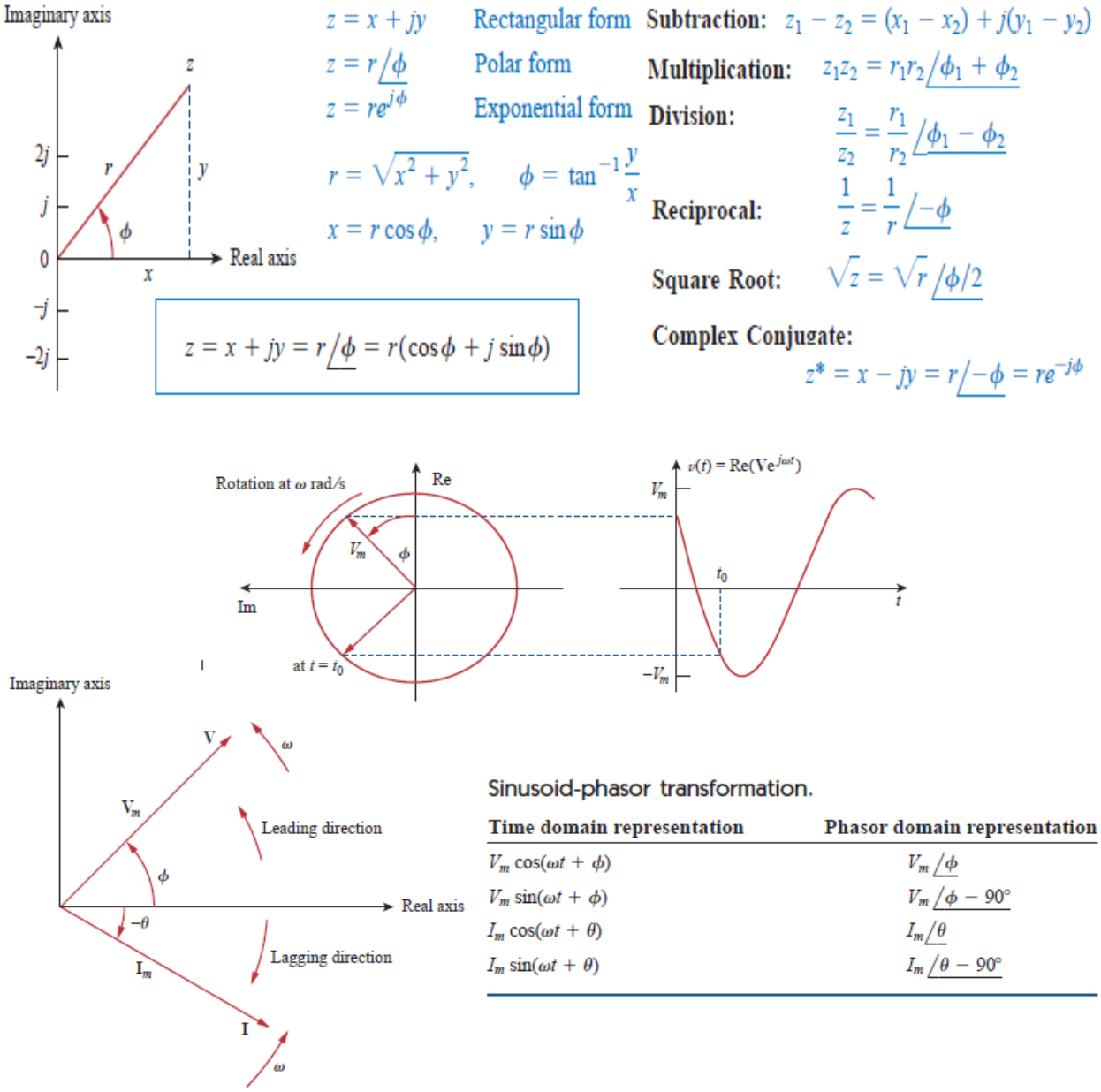


Fig. 4.1: Sinusoidal wave properties

A phasor is a complex number that represents the amplitude and phase of a sinusoid. The properties of phasors are presented in figure 4.2.



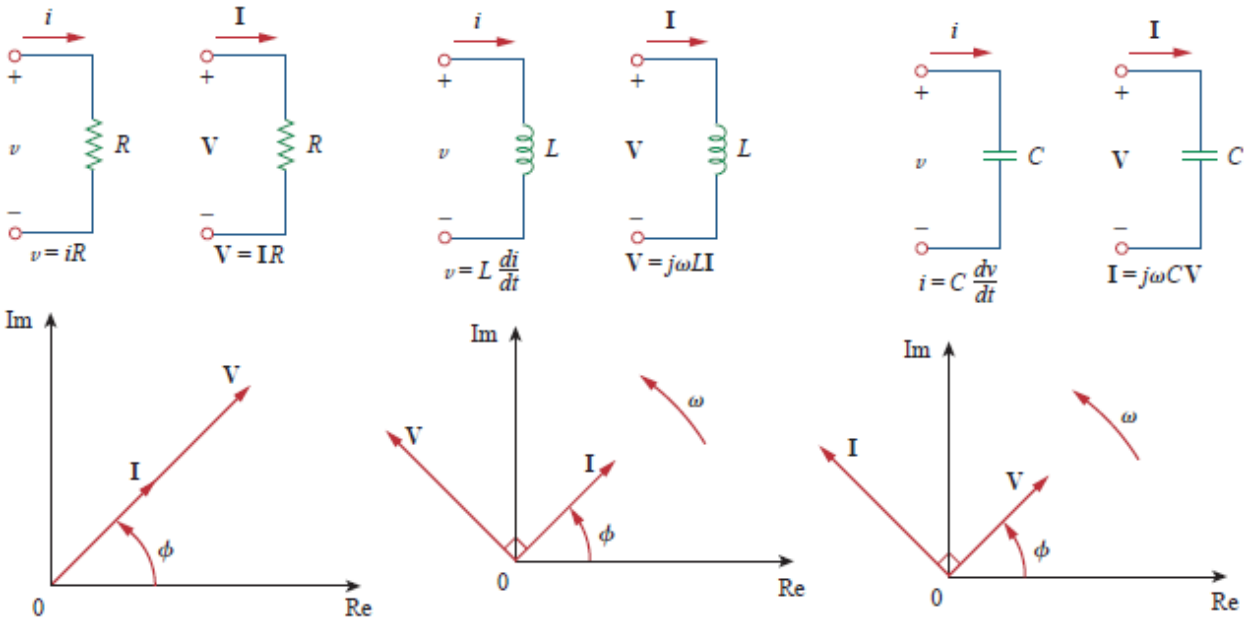
Sinusoid-phasor transformation.

Time domain representation	Phasor domain representation
$V_m \cos(\omega t + \phi)$	$V_m\angle\phi$
$V_m \sin(\omega t + \phi)$	$V_m\angle\phi - 90°$
$I_m \cos(\omega t + \theta)$	$I_m\angle\theta$
$I_m \sin(\omega t + \theta)$	$I_m\angle\theta - 90°$

Fig. 4.2: phasor properties

4.2 Electrical circuit analysis

Phasor relationships of circuit elements are summarized in figure 4.3



Summary of voltage-current relationships.

Element	Time domain	Frequency domain
R	$v = Ri$	$\mathbf{V} = R\mathbf{I}$
L	$v = L\frac{di}{dt}$	$\mathbf{V} = j\omega L\mathbf{I}$
C	$i = C\frac{dv}{dt}$	$\mathbf{V} = \frac{\mathbf{I}}{j\omega C}$

Fig. 4.3: Phasor relationships of circuit elements

Now we can solve any problem from chapter 2 contains R, L and C, if we have its impedance not resistance only that is meaning real and imaginary (we can use nodal and mesh analysis, source transform, superposition, thevenin and norton) for example in figure 4.4.

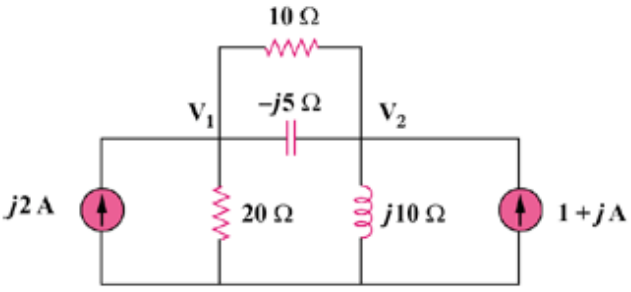
4.3 Average and RMS

The two important parameter in electronics calculations is average and root mean square value which are discussed here.

$$v_{avg} = \frac{1}{T}\int_0^T v(t)dt$$

Given a periodic function , its rms value (or the effective value) is given by

$$v_{rms} = \sqrt{\frac{1}{T}\int_0^T v^2(t)dt}$$



At node 1,

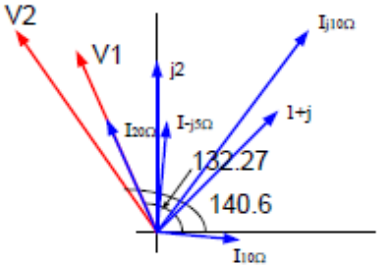
$$j2 = \frac{V_1}{20} + \frac{V_1 - V_2}{10} + \frac{V_1 - V_2}{-j5}$$

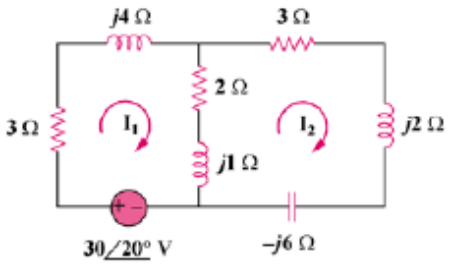
$$j40 = (3 + j4)V_1 - (2 + j4)V_2$$

At node 2,

$$\frac{V_1 - V_2}{10} + \frac{V_1 - V_2}{-j5} + 1 + j = \frac{V_2}{j10}$$

$$10(1 + j) = -(1 + j2)V_1 + (1 + j)V_2$$





For mesh 1,

$$(5 + j5)I_1 - (2 + j)I_2 - 30\angle 20° = 0$$

$$30\angle 20° = (5 + j5)I_1 - (2 + j)I_2 \quad (1)$$

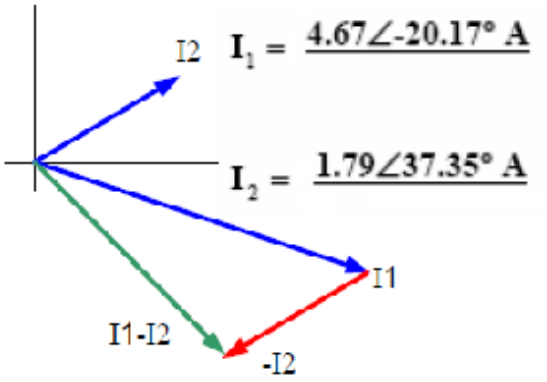
For mesh 2,

$$(5 + j3 - j6)I_2 - (2 + j)I_1 = 0$$

$$0 = -(2 + j)I_1 + (5 - j3)I_2 \quad (2)$$

$V_1 = \underline{22.87\angle 132.27° \text{ V}}$

$V_2 = \underline{27.87\angle 140.6° \text{ V}}$



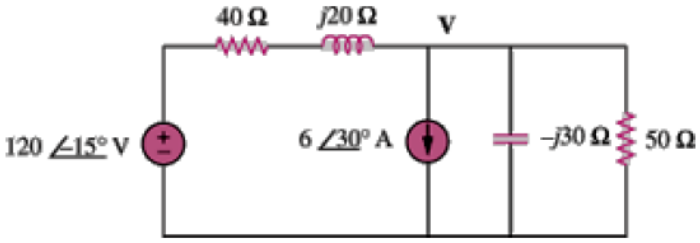
$I_1 = \underline{4.67\angle -20.17° \text{ A}}$

$I_2 = \underline{1.79\angle 37.35° \text{ A}}$

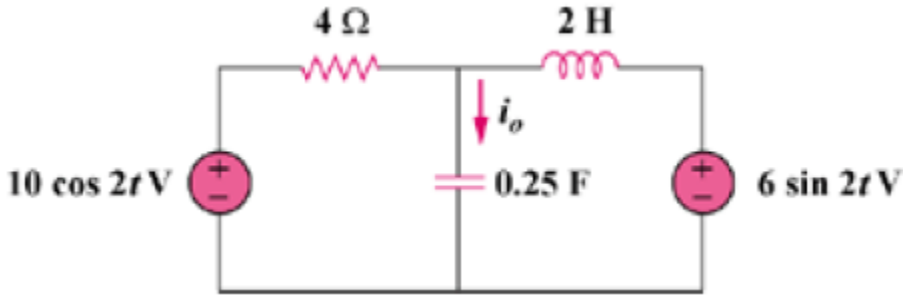
Fig. 4.4: Example on circuit analysis with R, L and C

4.4 Sheet 4

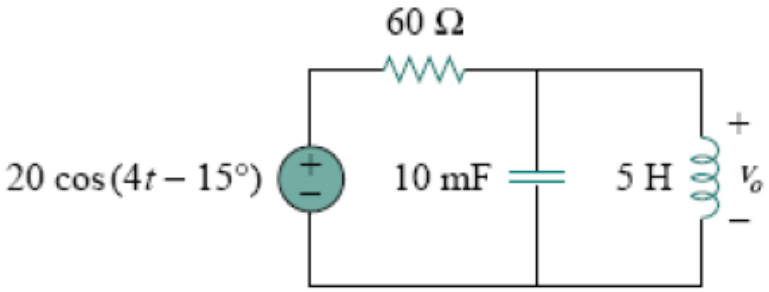
1.Use nodal analysis to find V in the circuit



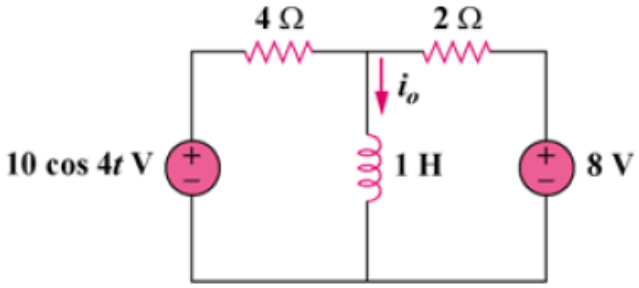
2.Solve for i_o in the following figure using mesh analysis.



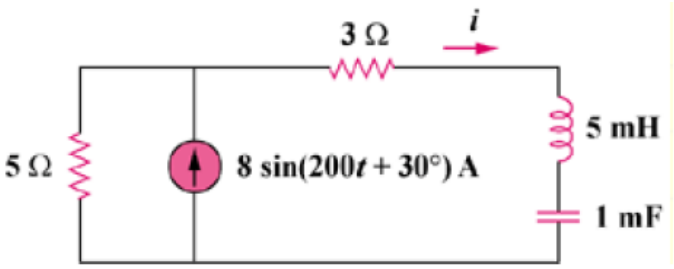
3.Determine v_0 in the circuit in the following figure



4.Find i_o in the circuit shown by using superposition.



5.Using source transformation, find i in the circuit



CHAPTER 5

INTRODUCTION OF SEMICONDUCTORS

CHAPTER 5

INTRODUCTION OF SEMICONDUCTORS

5.1 Fundamentals of atoms

5.1.1 Definitions of atom:

The atom is considered the smallest particle of the element. In addition to it is retaining the characteristics of matter such as if the atom was conductor for example, the matter of it must be conductor too. Finally, we can say that any atom has unique description. As shown in Fig. 5.1, Bohr model was describing the atomic structure

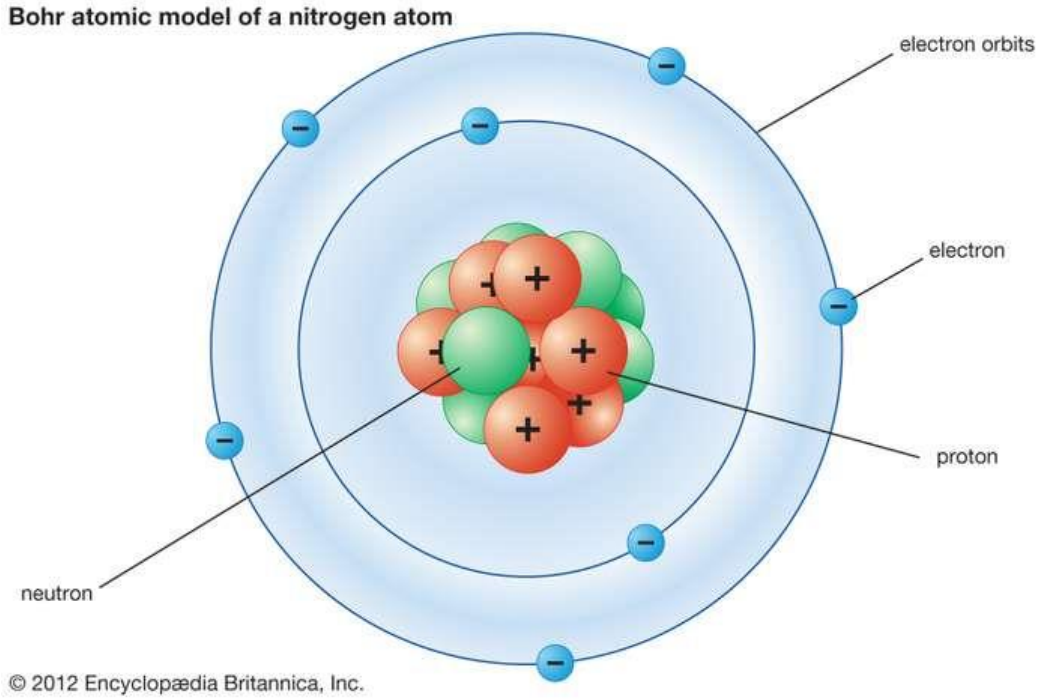


Fig. 5.1: Bohr model for atomic structure

5.1.2 Atomic number and Atomic weight

We can describe the atomic number by number of electrons or number of protons at the neutral state. In addition to describe atomic weight by number of electrons or number of protons plus number neutrons at the neutral state

5.1.3 Orbits and shells

The electrons orbits around the nucleus. Each electron orbits in the specified orbit. Each orbit has fixed energy level. The energy of orbit is increasing with increasing the radius of the orbit. Some of orbits complete shell. In contrast that, we have big difference between orbit and shell. In the view of shell, each atom has fixed number of shell. Each shell has maximum number of electrons. The energy gap between two shell is larger than energy gap between two orbits at the same shell.

5.2 Basic of materials

To classify the materials according to their conductivity we must first define the main parameter in material which is called resistivity**.**

5.2.1 Resistivity

We can define the resistivity as resistance of matter against flow the electrical current. Now the differences between materials will be stated in the following subsection.

5.2.2 Insulators, semiconductors and conductors

As shown in Fig. 5.2, The material will be classified into three type according to its resistivity by energy diagram as the following:

- Insulators: this type contain wide energy gap between valence band and conduction band. Its conduction band hasn't any of free electrons. Its valence band contains very few valence electrons. The valence electron needs high work function to transfer from valance band to conduction band.
- Semiconductors: this type contain energy gap between valence band and conduction band but narrow than in insulators. Its conduction band has few number of free electrons. Its valence band contains few valence electrons. The valence electron needs moderate work function to transfer from valance band to conduction band.
- Conductors: this type contain overlapping between valence band and conduction band. The free electrons is exist already in conduction band. Its valence band contains high numbers of

valence electrons. The valence electron needs small work function to transfer from valance band to conduction band.

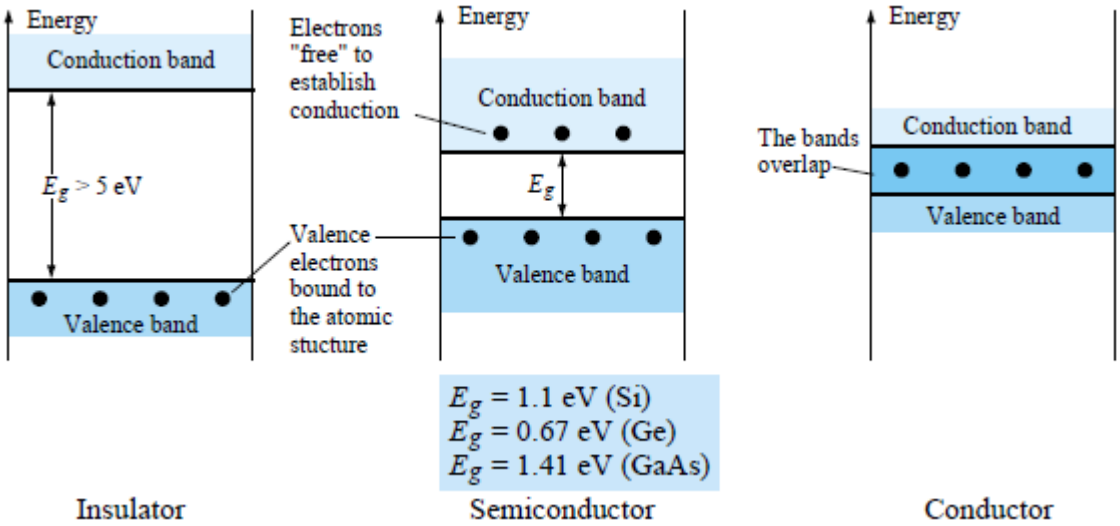


Fig. 5.2: Energy diagram for (a)Insulators, (b)Semiconductors and (c)conductors

5.3 Semiconductor concepts

As shown in Fig. 5.3, the intrinsic semiconductor is obtained. The more popular semi conductor materials are Silicon (Si) which has 14 electrons and germanium (Ge) which has 32 electrons. All semiconductors have 4 electrons at the Fermi level.

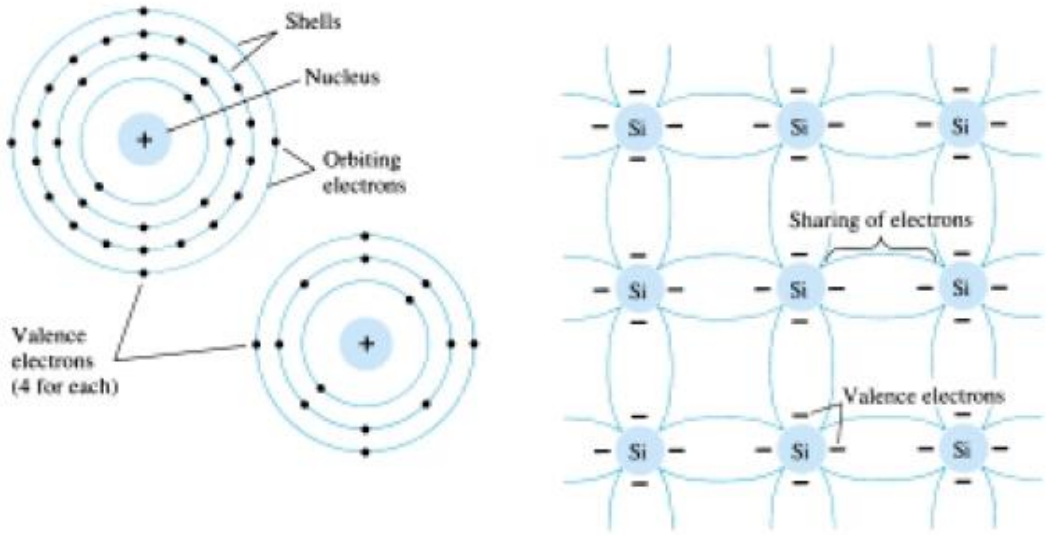


Fig. 5.3: Intrinsic semiconductor.

5.3.1 Doping process

The doping is control process by adding impurities to pure semiconductors to enhance its conductivity to electrical current.

5.3.2 N-type material

This type is negative type with majority of electrons and minority of holes. The doping in this type is happened by pentavalent atom which has five electrons in the Fermi level. Four of them complete covalent bonds and still one free electron to conduct electrical current as shown in Fig. 5.4.

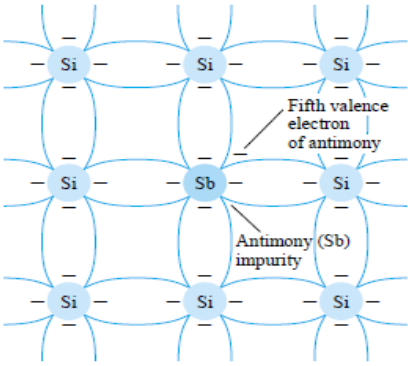


Fig. 5.4: N-type material.

5.3.3 P-type material

This type is positive type with majority of holes and minority of electrons. The doping in this type is happened by trivalent atom which has three electrons in the Fermi level. all of them complete covalent bonds and still one hole need one free electron to conduct electrical current as shown in Fig. 5.5.

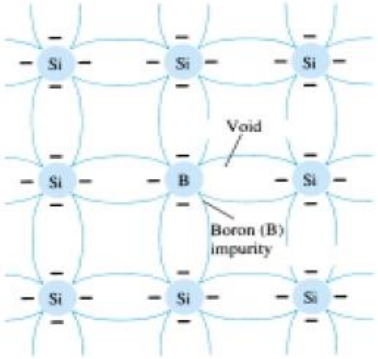


Fig. 5.5: P-type material.

5.3.4 Depletion layer

First, we will put N-type material beside P-type material. The diffusion of electrons will be happened from N-type to P-type. The second step is the recombination between electrons and holes to complete electron and hole pairs. The third step is the ionization which makes the N-type change from neutral state to positive ions (Donors atoms) and the P-type change from neutral state to negative ions (Acceptors atoms). At the equilibrium between the attraction force between positive ions and electrons and the repulsion force between negative ions and electrons complete the depletion layer as shown in Fig. 5.6.

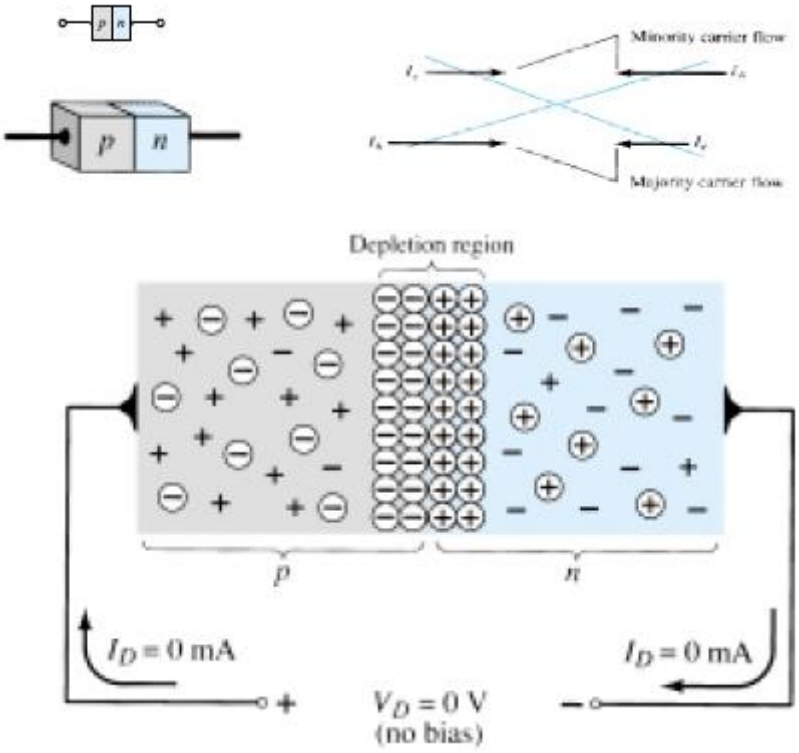


Fig. 5.6: PN junction.

5.3.5 Barrier potential

This potential represent the depletion layer or depletion region and it is equal to 0.7 in Si and 0.3 in Ge.

5.3.6 Forward bias and reverse bias

As shown in Fig. 5.7, the biasing in the PN junction which is called diode is classified into two types as the following:

- **Forward bias (F.B):** the connection is positive DC battery with P-type and negative DC battery with N-type generate two repulsion force between them then depletion region width is reduced then flow the electrical current I_D.

$$I_D = I_s(e^{\frac{kV_d}{T_k}} - 1) \quad (5\text{-}1)$$

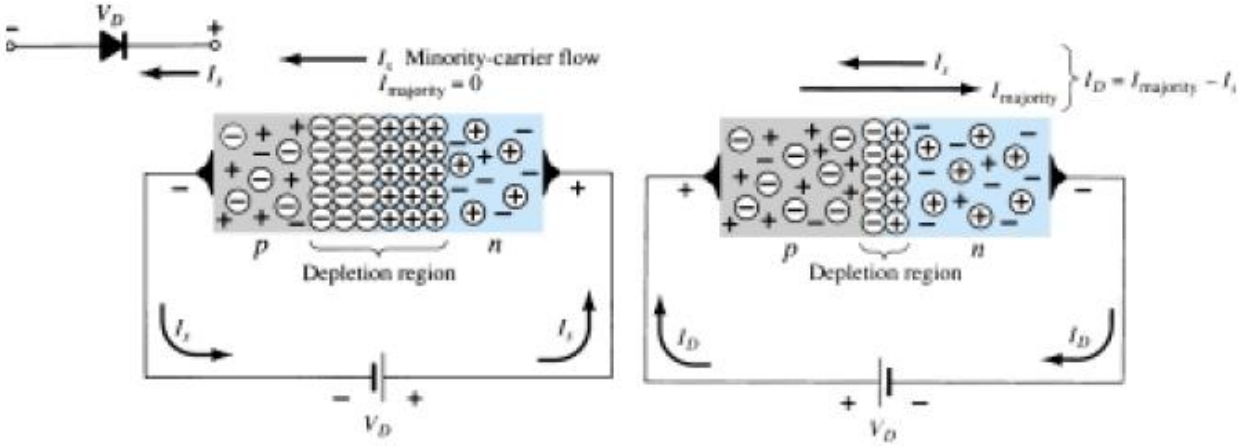
where:

V_d: Voltage on diode.

k: 11,600/η with η = 1 for Ge and η = 2 for Si.

T_k: T_C + 273.

- **Reverse bias (R.B):** the connection is positive DC battery with N-type and negative DC battery with P-type generate two attraction force between them then depletion region width is increased then no flow the electrical current or flow small reverse saturation current I_s.



(a) R.B (b) F.B

Fig. 5.7: Diode biasing.

5.3.7 Electronic and hole currents

The electron current generates the electrical current at the against direction. In addition to, the hole current generates the electrical current at the same direction.

5.4 Sheet 5

1. Define an Atom?
2. What is the difference between atomic number and mass number?
3. What is the difference between orbit and shell?
4. Define the resistivity?
5. What are the differences between conductor, insulators and semiconductor?
6. Define doping process?
7. How N-type is created?
8. How P-type is created?
9. How Depletion layer (region) is created, then define the barrier potential?
10. What are the differences between forward and reverse biasing?
11. What is the difference between electron and hole currents?

CHAPTER 6

DIODE AND ITS APPLICATIONS

CHAPTER 6

DIODE AND ITS APPLICATIONS

6.1 Introduction of diode

We can show the characteristics curve for diode can be presented as shown in Fig. 6.1 but first we will present all models diode to arrive it.

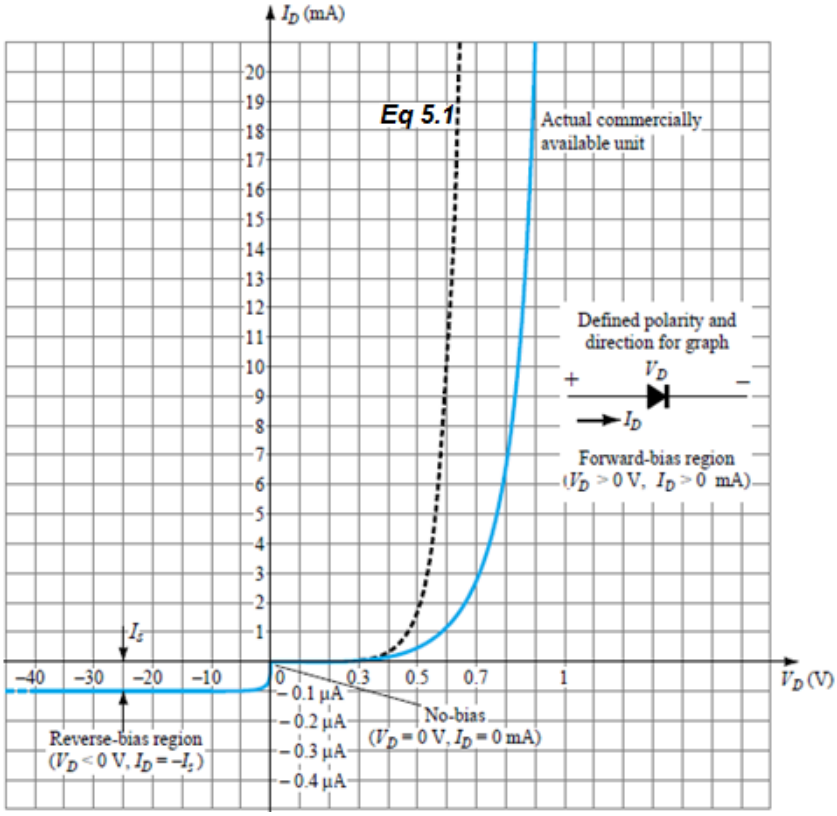


Fig. 6.1: Characteristics curve for Si diode.

6.2 models of diode

6.2.1 ideal model

As shown in Fig. 6.2, this model make diode as short circuit when is connected as F.B and open circuit when connected at R.B.

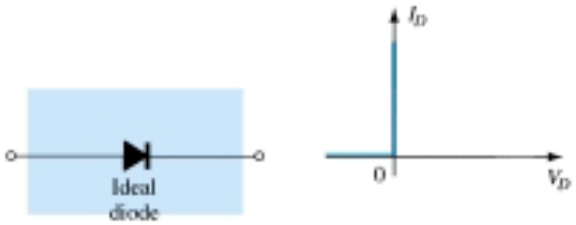


Fig. 6.2: Ideal model.

6.2.2 Barrier constant model

As shown in Fig. 6.3, this model make diode as Battery when is connected as F.B and open circuit when connected at R.B.

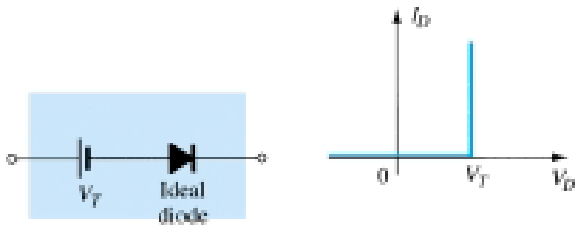


Fig. 6.3: Barrier potential (constant) model.

6.2.3 Linear model

As shown in Fig. 6.4, this model make diode as battery with resistor when is connected as F.B and open circuit when connected at R.B.

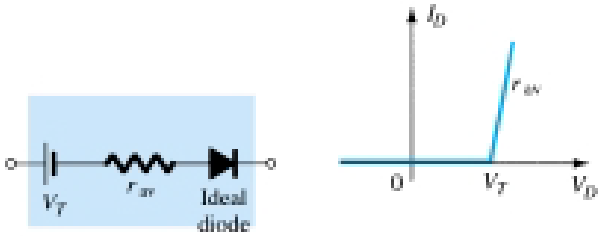


Fig. 6.4: Linear (piecewise) model.

6.2.4 Actual model

As shown in Fig. 6.5, this model make diode as battery with resistor when is connected as F.B and high resistor when connected at R.B.

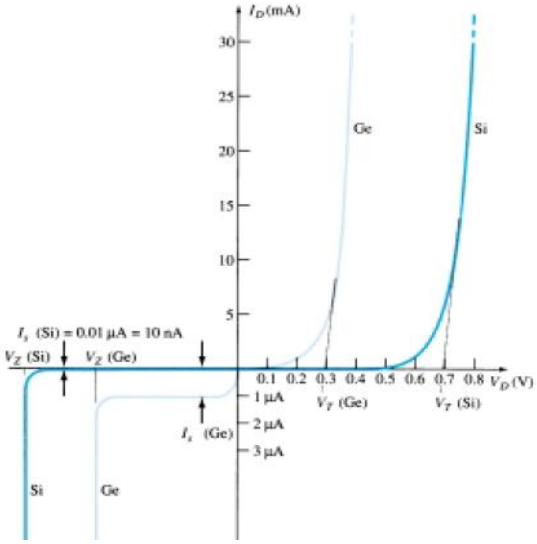


Fig. 6.5: Actual (Practical) model.

6.3 Applications of diode

6.3.1 DC applications of diode

We use the section 6.2 to solve any problem here such as the following example:

Example 6.1: For the series diode configuration of Fig. 6.6 (a) employing the diode characteristics of Fig. 6.6 (b) determine:

a) V_{dQ} and I_{dQ}.

b) V_R.

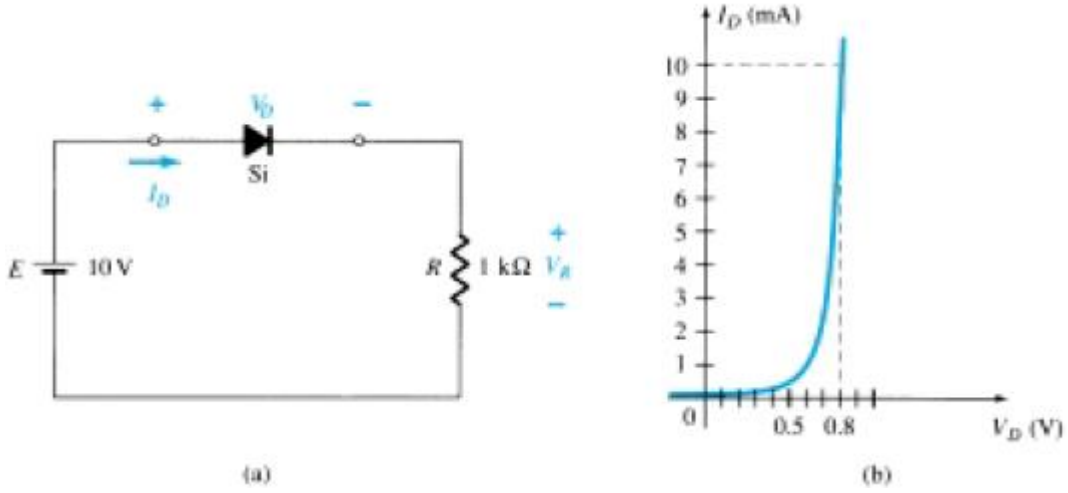


Fig. 6.6: Example 6.1.

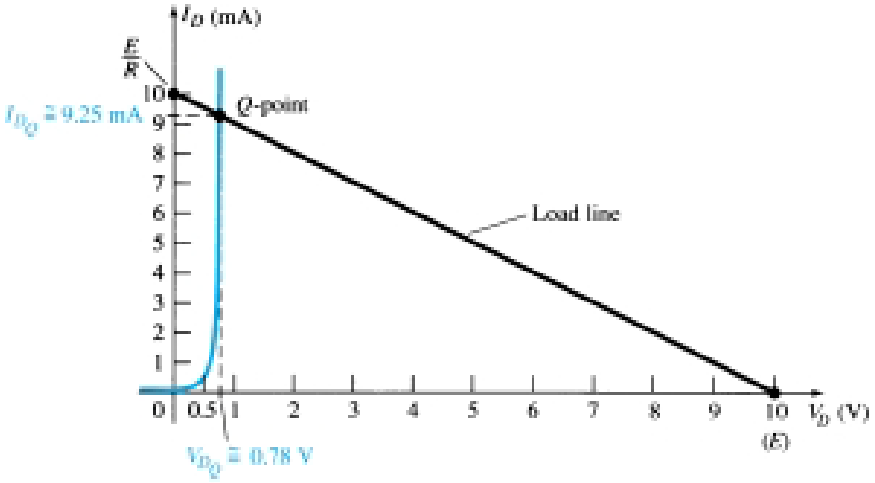
Solution:

By graph

$$I_D(at\ V_D = 0) = \frac{E}{R} = 5\ mA$$

$$V_D(at\ I_D = 0) = E = 10\ V$$

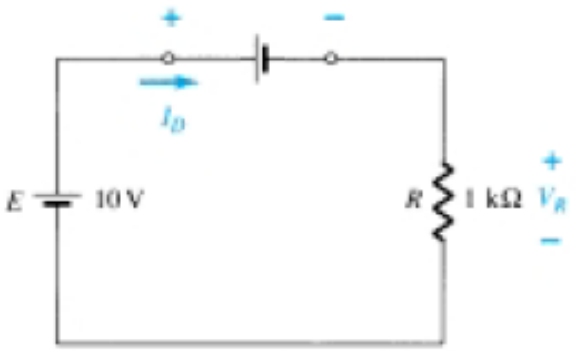
draw load line



$V_{dQ} = 0.78\ V$ and $I_{dQ} = 9.25\ mA$.

$V_R = E - V_{dQ}$ =9.22 V or
$V_R = R * I_{dQ} = 9.25$ V

without graph



Diode (F.B)
Assume constant model: $V_{dQ} = 0.7$V and I_{dQ}= 10-0.7/1 K= 9.3 mA.
$V_R = E - V_{dQ} = R * I_{dQ} = 9.3$ V

6.3.2 AC applications of diode

We will present two main application in this subsection such as the following:

- **Half wave rectifier (HWR):**

Here we put time analysis in our vision as shown in Fig. 6.7 (a). The input sinusoidal wave enter to diode to half of it pass and diode prevent another half. To know how we do that, we will analyze the circuit:

1. Assume ideal model.
2. At positive half cycle:
   Diode (F.B).
   $V_o = V_i$.
   output signal is shown in Fig. 6.7 (b).
3. At negative half cycle:
   Diode (F.B).
   $V_o = 0$ V.
   output signal is shown in Fig. 6.7 (c).
4. The effect of barrier potential on HWR is shown in Fig. 6.7 (d).
5. The average voltage equal to $V_{DC} = V_{avg} = \frac{V_m}{\pi}$ as shown in Fig. 6.7 (e).
6. Peak inverse voltage PIV = $V_K - V_A(when\ Diode\ off) = V_m$.

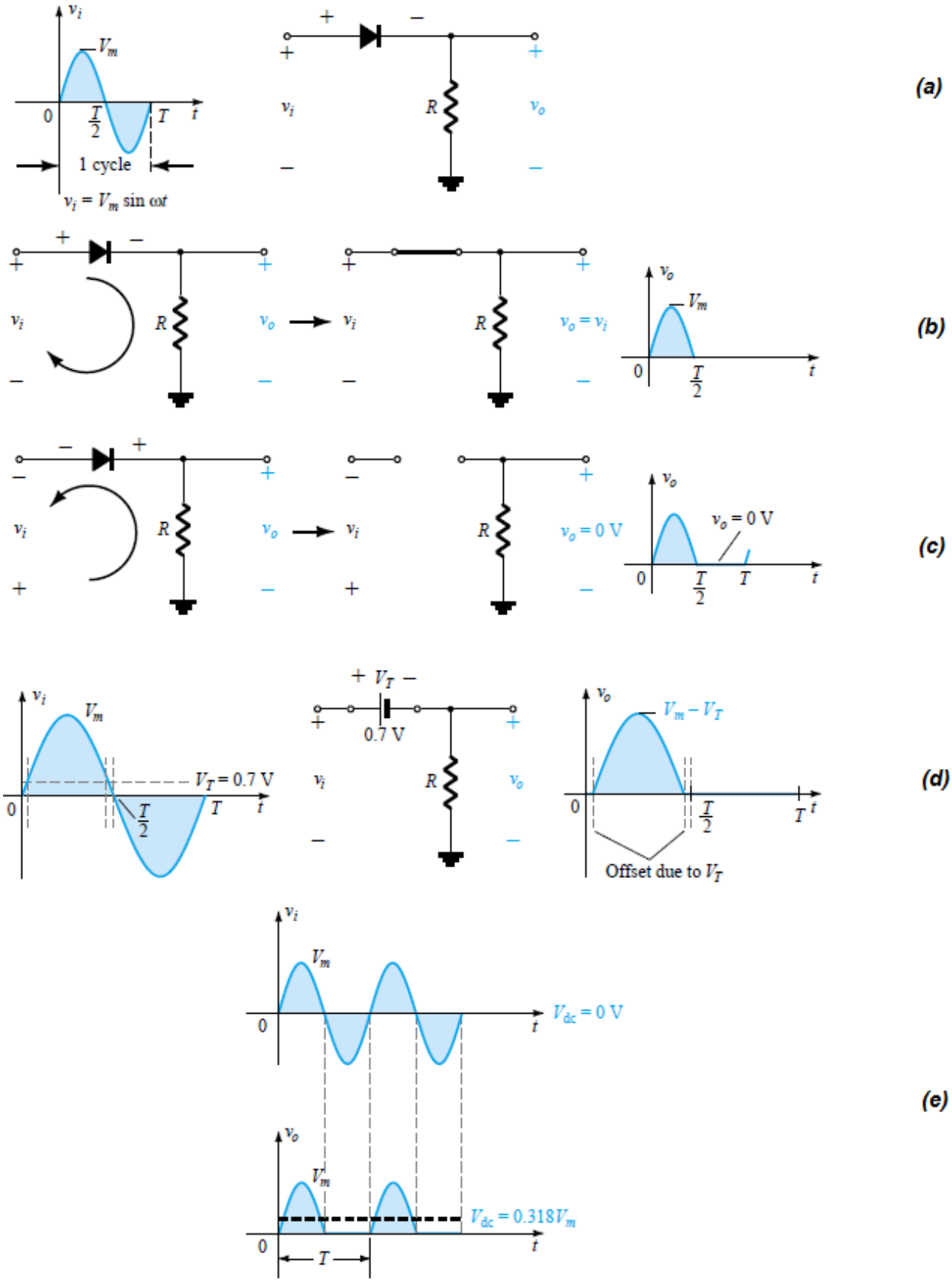


Fig. 6.7: HWR circuit.

- **Full wave rectifier (FWR):**

Here we put time analysis in our vision as shown in Fig. 6.8 (a) and Fig. 6.9 (a). The input sinusoidal wave enter to diode to half of it pass as it is and diode reverse another half from negative to positive such as example. We can classify the full wave rectifier to two types:

Center-Tapped transformer FWR

To know how we do that, we will analyze the circuit:

1. Assume ideal model and
2. (V at secondary = V at primary * Number of secondary turns/ number of primary turns).
3. At positive half cycle:
   D1 (F.B) and D2(R.B).
   $V_o = V_i$.
   output signal is shown in Fig. 6.8 (b).
4. At negative half cycle:
   D2 (F.B) and D1(R.B).
   $V_o = V_i$.
   output signal is shown in Fig. 6.8 (c).
5. The average voltage equal to $V_{DC} = V_{avg} = \frac{2*V_m}{\pi}$.
6. Peak inverse voltage
   PIV = $V_K - V_A(when\ Diode\ off) = 2V_m$ as shown in Fig. 6.8 (d).

7. The effect of barrier potential on FWR.

$V_o = V_i$ - V_T ($V_T = V_B$).

$$V_{DC} = V_{avg} = \frac{2 * (V_m - V_T)}{\pi}$$

PIV = $V_K - V_A(when\ Diode\ off) = 2V_m$-$V_T$

8. No turns ratio effect on FWR and barrier potential model.

$V_o = (V_i/2)$ - V_T ($V_T = V_B$).

$$V_{DC} = V_{avg} = \frac{2 * ((V_m/2) - V_T)}{\pi}$$

PIV = $V_K - V_A(when\ Diode\ off) = V_m$-$V_T$

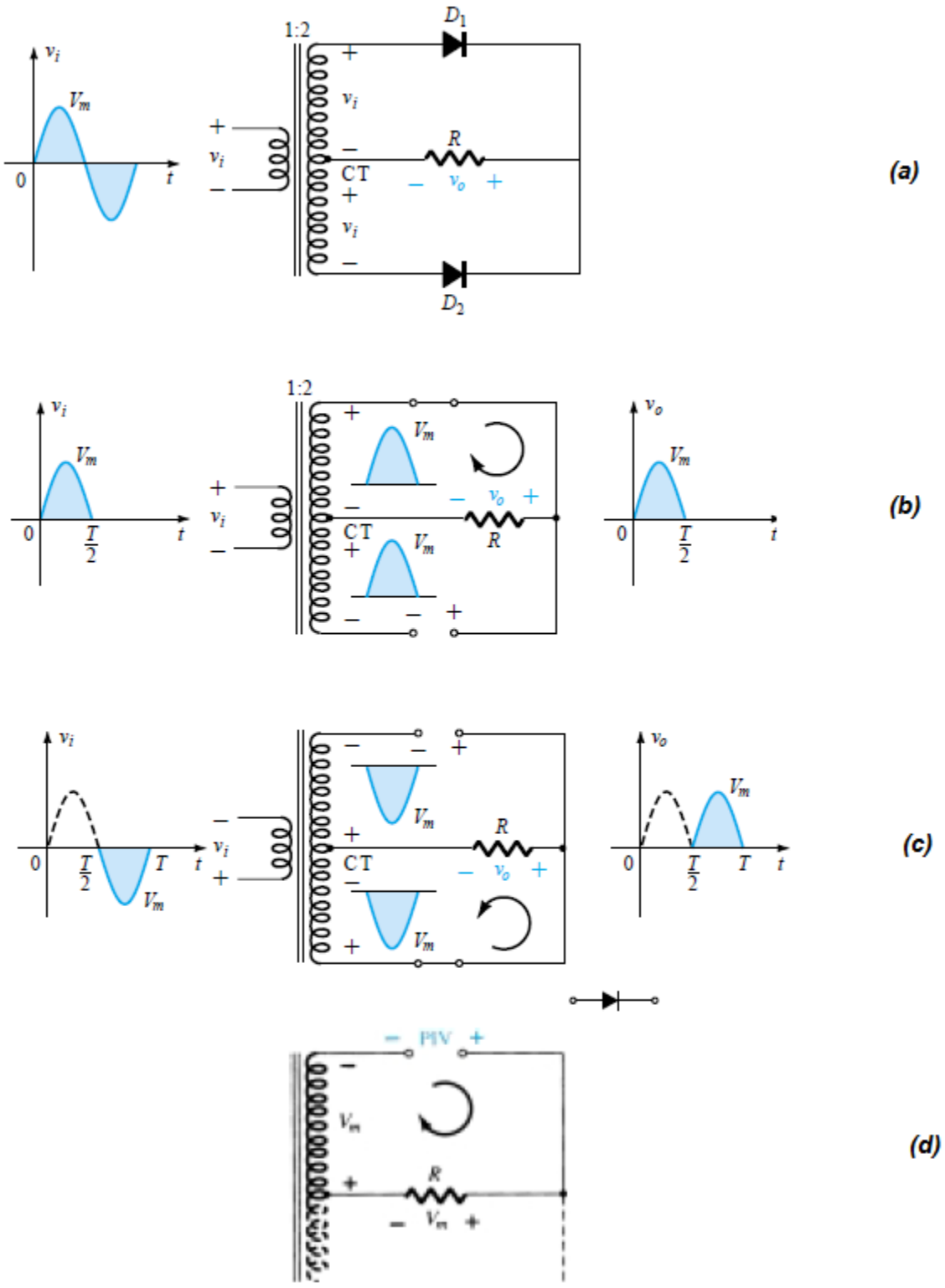


Fig. 6.8: Center-tapped circuit.

Bridge FWR

To know how we do that, we will analyze the circuit:

1. Assume ideal model.
2. At positive half cycle: D2, D3 (F.B) and D1, D4(R.B). $V_o = V_i$. output signal is shown in Fig. 6.9 (b).
3. At negative half cycle: D2, D3 (R.B) and D1, D4(F.B). $V_o = V_i$. output signal is shown in Fig. 6.9 (c).
4. The average voltage equal to $V_{DC} = V_{avg} = \frac{V_m}{\pi}$ as shown in Fig. 6.9 (e).
5. PIV = $V_K - V_A(when\ Diode\ off) = V_m$ as shown in Fig. 6.9 (f).
6. The effect of barrier potential on FWR as shown in Fig. 6.9 (d).

$V_o = V_i$ - $2V_T$ ($V_T = V_B$).

$$V_{DC} = V_{avg} = \frac{2 * (V_m - 2V_T)}{\pi}$$

PIV = $V_K - V_A(when\ Diode\ off) = V_m$-$V_T$

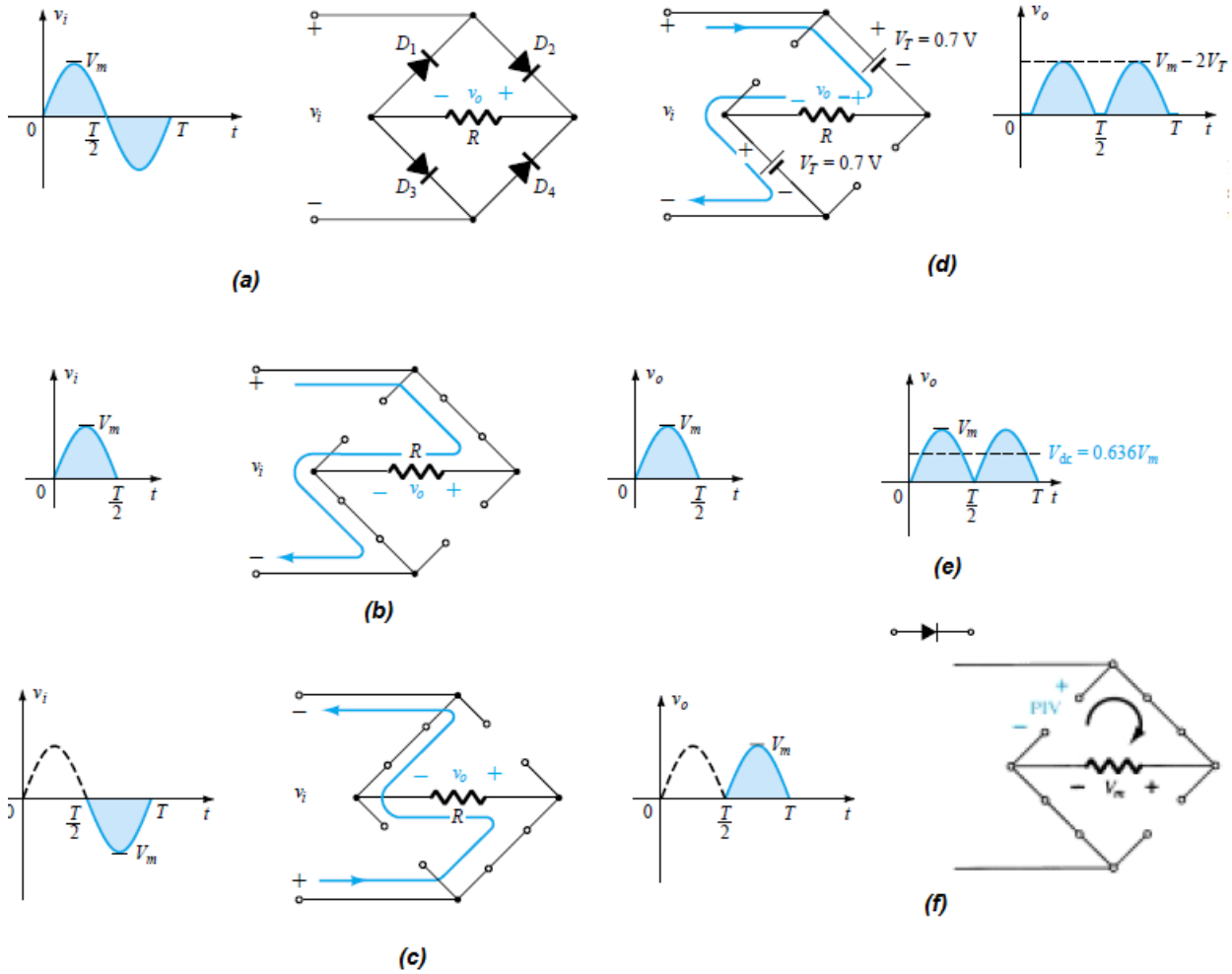
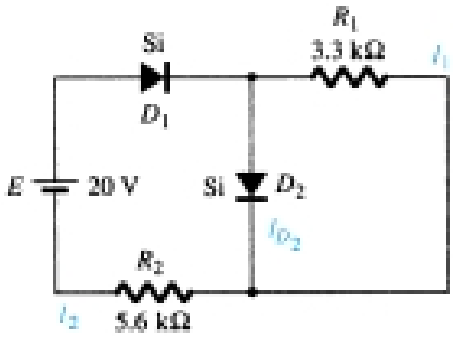


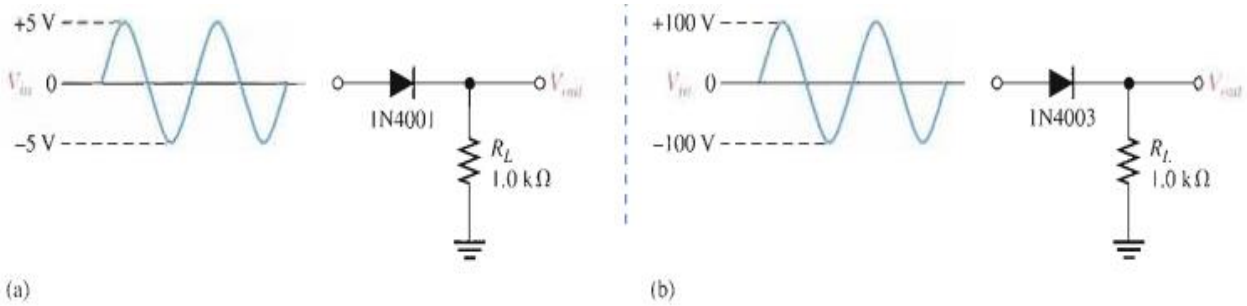
Fig. 6.9: Bridge circuit.

6.4 Sheet 6

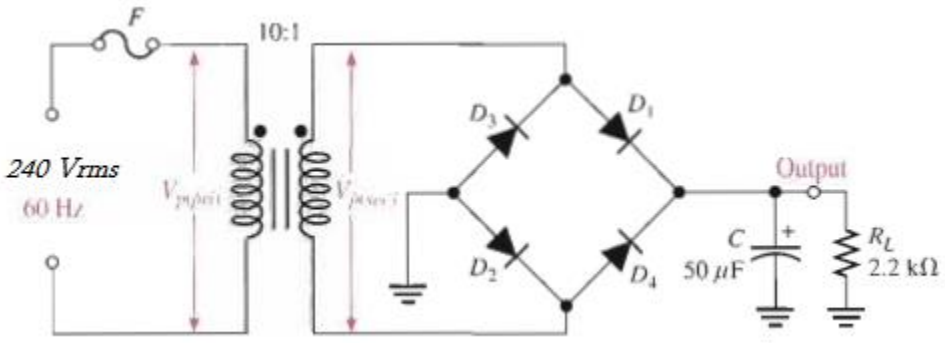
1. Describe the models of diode?
2. What is the difference between half wave rectifier and full wave rectifier in terms of PIV and average voltage?
3. Determine the currents of diodes in the following figure?



4. Draw the output voltages of each rectifier for the following figures?



5. Determine the output voltage and draw its waveform for the following figure, then calculate PIV and Vdc?



Chapter 7

Different Types of Transistors

Chapter 7

Different Types of Transistors

7.1 Introduction of Bipolar Junction Transistor (BJT)

During the period 1904–1947, the vacuum tube was undoubtedly the electronic device of interest and development. In 1904, the vacuum-tube diode was introduced by J. A. Fleming. Shortly thereafter, in 1906, Lee De Forest added a third element, called the control grid, to the vacuum diode, resulting in the first amplifier, the triode. In the following years, radio and television provided great stimulation to the tube industry. Production rose from about 1 million tubes in 1922 to about 100 million in 1937. In the early 1930s the four-element tetrode and five-element pentode gained prominence in the electron-tube industry. In the years to follow, the industry became one of primary importance and rapid advances were made in design, manufacturing techniques, high-power and high-frequency applications, and miniaturization.

On December 23, 1947, however, the electronics industry was to experience the advent of a completely new direction of interest and development. It was on the afternoon of this day that Walter H. Brattain and John Bardeen demonstrated the amplifying action of the first transistor at the Bell Telephone Laboratories. The original transistor (a point-contact transistor) is shown in Fig. 7.1. The advantages of these three terminal solid-state devices over the tube were immediately obvious: It was smaller and lightweight; had no heater requirement or heater loss; had rugged construction; and was more efficient since less power was absorbed by the device itself; it was instantly available for use, requiring no warm-up period; and lower operating voltages were possible. Note in the discussion above that this chapter is our first discussion of devices with three or more terminals. You will find that all amplifiers (devices that increase the voltage, current, or power level) will have at least three terminals with one controlling the flow between two other terminals.

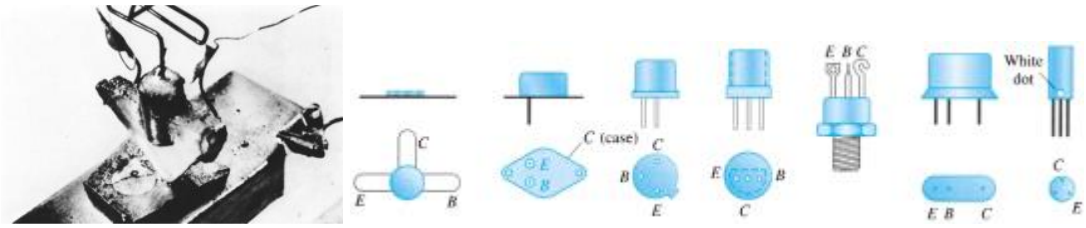


Fig. 7.1: The first transistor and others

7.1.1 BJT definition

We can describe the BJT as the following points:

- The BJT is an abbreviation for Bipolar Junction Transistor
- The BJT contains from three types of semiconductors material (2N&P or 2P&N)
- The BJT contains three terminals (Emitter (E) - Base (B)- Collector(C)). Note that the base doping is slightly than other terminals.

7.1.2 BJT construction, model and symbol

The planar structure for BJT is shown in fig 7.2. The main two types of BJT are NPN and PNP. We can obtain the difference between graph construction, modeling and symbols for these types as shown in Table 7.1.

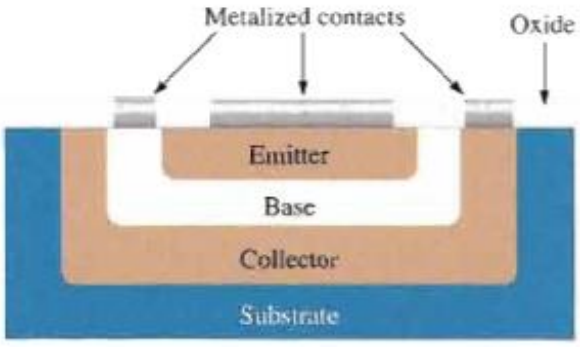
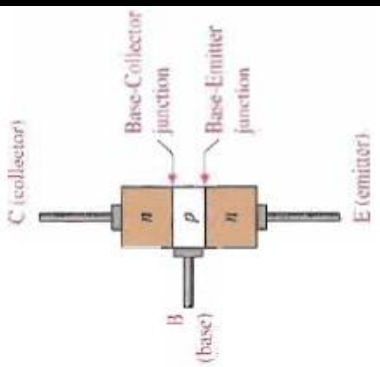
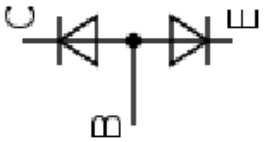
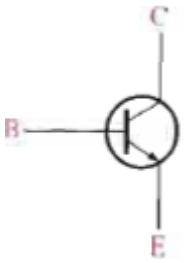
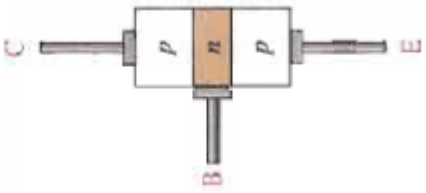
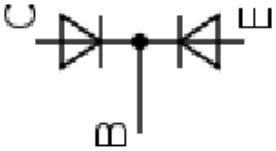
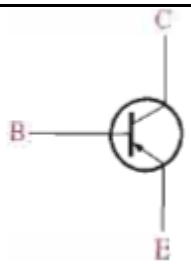


Fig. 7.2: The BJT structure planar

Table 7.1: The BJT graph construction, modeling and symbols

BJT types	Constructions	Models	Symbols
NPN			
PNP			

7.1.3 BJT operations

As shown in the previous subsection any BJT contains from two diodes with two junctions which called BCJ between base and collector and BEJ between base and emitter. According that we can classified operations and applications of BJT as shown in table 7.2.

Table 7.2: The BJT modes

BEJ	BCJ	Operation mode	Application
Forward bias	Forward bias	Saturation	Switch on
Forward bias	Reverse bias	Active	Amplifier
Reverse bias	Forward bias	Reverse Active	Digital electronics
Reverse bias	Reverse bias	Cutoff	Switch off

Now we can go to one of the important applications for the BJT which called an amplifier device. In this paragraph, we will describe how the BJT operate as amplifier

device. As shown in figure 7.3, the following steps are happened to operate the BJT as an amplifier:

- Operate BJT in active mode by making BEJ forward bias and BCJ reverse bias as shown in figure 7.3.
- The electrons will repulsion with negative terminal of DC battery.
- Some of electron combined with small number of holes in base then generate base current in opposite direction I_B.
- The reminder of electrons will be continue with electrons from collector and go to the positive terminal which connected by collector then generate collector current in opposite direction I_B.
- $I_C \gg I_B$ and Current gain is called $\beta = I_C/I_B$ and $I_E = I_C + I_B$ we can define $\alpha = I_C/I_E$
- Then we can say the relations between transistor currents $I_C = \beta I_B$, $I_E = (1 + \beta)I_B$ and $\alpha = \frac{\beta}{1+\beta}$

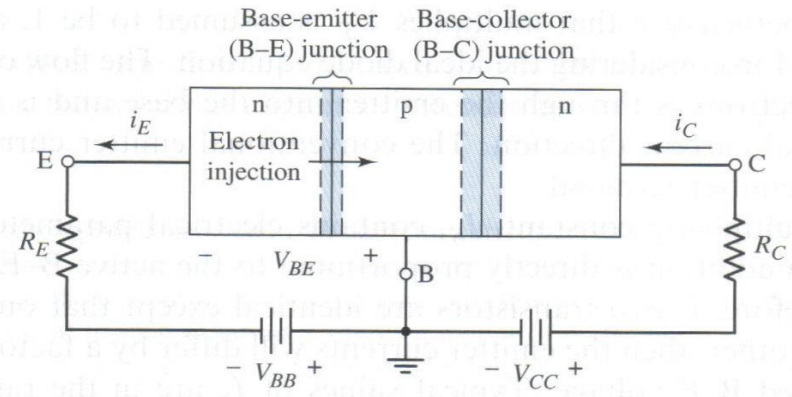


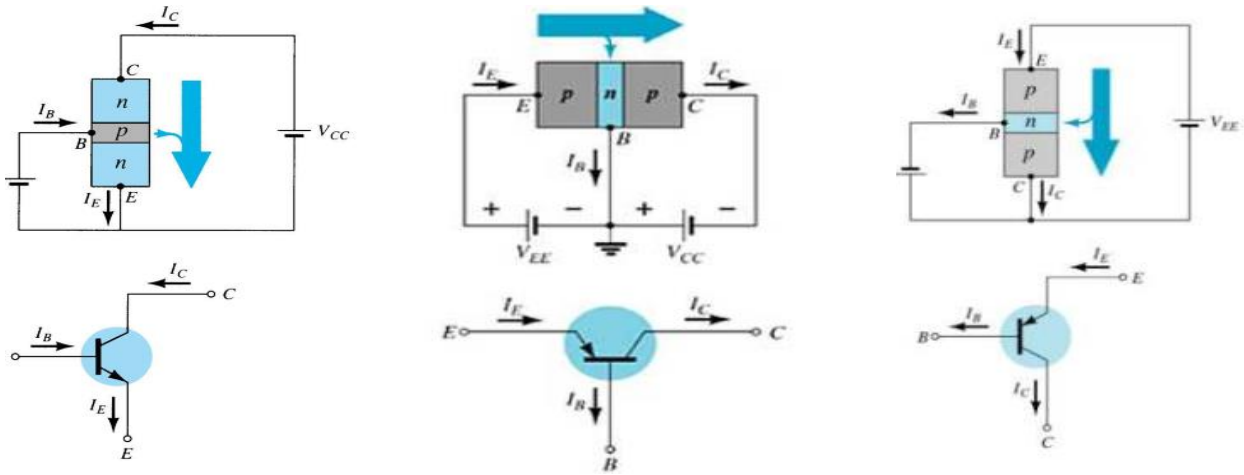
Fig. 7.3: The BJT as amplifier

7.1.4 BJT configurations

The configurations of BJT are three types according to connection input and output as shown in the following table 7.3 and figure 7.4.

Table 7.3: The BJT configurations.

Configuration type	Input terminal	Output terminal
Common emitter	Base	Collector
Common base	Emitter	Collector
Common collector (emitter follower)	Base	Emitter



a. common emitter b. common base c. common collector

Fig 7.4: BJT configurations

7.1.5 BJT characteristics curves

In this subsection, we will present the characteristics curves of BJT. As shown in figure 7.5. the input and output characteristics curves.

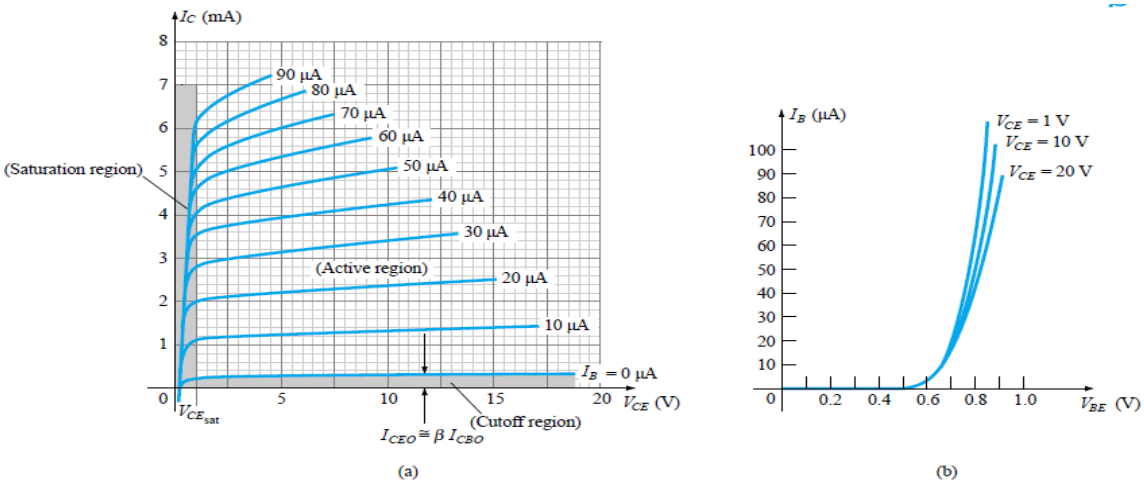


Fig. 7.5: The Characteristics of a silicon transistor in the common-emitter configuration: (a) collector characteristics; (b) base characteristics.

7.1.6 DC Biasing

We will study the NPN BJT common emitter configuration. There are three types of biasing circuit:

- ❑ Fixed-bias circuit
- ❑ Emitter-stabilized bias circuit
- ❑ Voltage divider bias circuit
- ❑ DC bias with voltage feedback

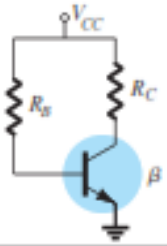
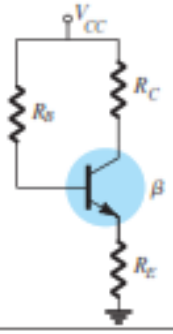
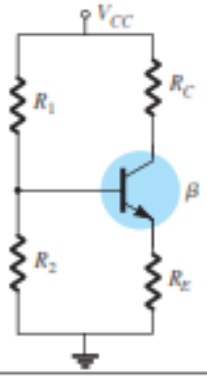
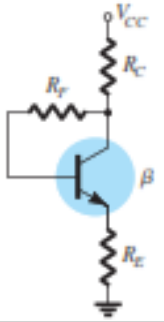
i. The main steps for DC analysis

To do DC analysis for any circuit for BJT, we state the following steps:

- Assume the transistor in active mode $V_{BE} = 0.7$ and BCJ reverse.
- Make Kirchhoff's law on input loop and must be a cross between E and B terminals. Then find all currents in circuits.
- Make Kirchhoff's law on output loop and must be a cross between E and C terminals. Then find all currents in circuit.
- find β and α.
- Check on BCJ if it is in reverse the BJT will be in active mode and assumption is true. If not, assume transistor in saturation mode and make $V_{CE} = 0.2$ and find I_C from output loop, then we will do an input loop to calculate all voltages and currents in circuit.
- From output loop, make current equal zero and find V_{CE} and another time make $V_{CE} = 0$ find I_C then from these two points draw a DC loadline which intersect with an output characteristic curve in Q point which called operating point.

Table 7.4 shows the circuit and analysis different types of DC biasing.

Table 7.4: DC biasing circuits

Type	Configuration	Pertinent Equations
Fixed-bias		$I_B = \frac{V_{CC} - V_{BE}}{R_B}$ $I_C = \beta I_B, I_E = (\beta + 1)I_B$ $V_{CE} = V_{CC} - I_C R_C$
Emitter-bias		$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$ $I_C = \beta I_B, I_E = (\beta + 1)I_B$ $R_i = (\beta + 1)R_E$ $V_{CE} = V_{CC} - I_C(R_C + R_E)$
Voltage-divider bias		EXACT: $R_{Th} = R_1 \| R_2, E_{Th} = \frac{R_2 V_{CC}}{R_1 + R_2}$ $I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E}$ $I_C = \beta I_B, I_E = (\beta + 1)I_B$ $V_{CE} = V_{CC} - I_C(R_C + R_E)$ APPROXIMATE: $\beta R_E \geq 10R_2$ $V_B = \frac{R_2 V_{CC}}{R_1 + R_2}, V_E = V_B - V_{BE}$ $I_E = \frac{V_E}{R_E}, I_B = \frac{I_E}{\beta + 1}$ $V_{CE} = V_{CC} - I_C(R_C + R_E)$
Collector-feedback		$I_B = \frac{V_{CC} - V_{BE}}{R_F + \beta(R_C + R_E)}$ $I_C = \beta I_B, I_E = (\beta + 1)I_B$ $V_{CE} = V_{CC} - I_C(R_C + R_E)$

7.1.6. AC ANALYSIS FOR BJT

a.BJT Transistor Modeling

- A model is an equivalent circuit that represents the AC characteristics of the transistor.
- A model uses circuit elements that approximate the behavior of the transistor.
- There are two models commonly used in small signal AC analysis of a transistor:
  - re model
  - Hybrid equivalent model

❑ The re Transistor Model

- BJTs are basically current-controlled devices; therefore, the re model uses a diode and a current source to duplicate the behavior of the transistor.
- One disadvantage to this model is its sensitivity to the DC level. This model is designed for specific circuit conditions.

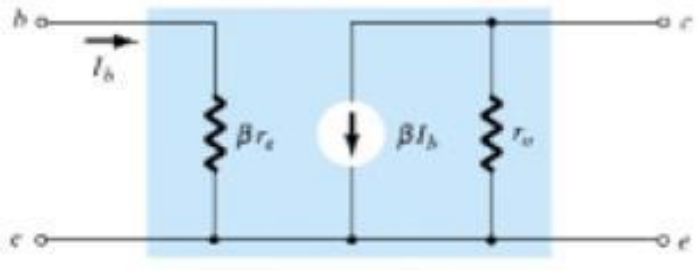


Fig 7.6: re Transistor Model

7.2 Basics of Field Effect Transistors (FET)

7.2.1 FET overview

The field-effect transistor (FET) is a three-terminal device used for a variety of applications that match, to a large extent, those of the BJT transistor described in previous section. Although there are important differences between the two types of devices, there are also many similarities that will be pointed out in the sections to follow. The primary difference between the two types of transistors is the fact that the BJT

transistor is a current-controlled device as depicted in Fig.7.7 a, while the JFET transistor is a voltage-controlled device as shown in Fig.7.7 b. In other words, the current I_C in Fig.7 a is a direct function of the level of I_B. For the FET the current I will be a function of the voltage V_{GS} applied to the input circuit as shown in Fig.7b. In each case the current of the output circuit is being controlled by a parameter of the input circuit—in one case a current level and in the other an applied voltage.

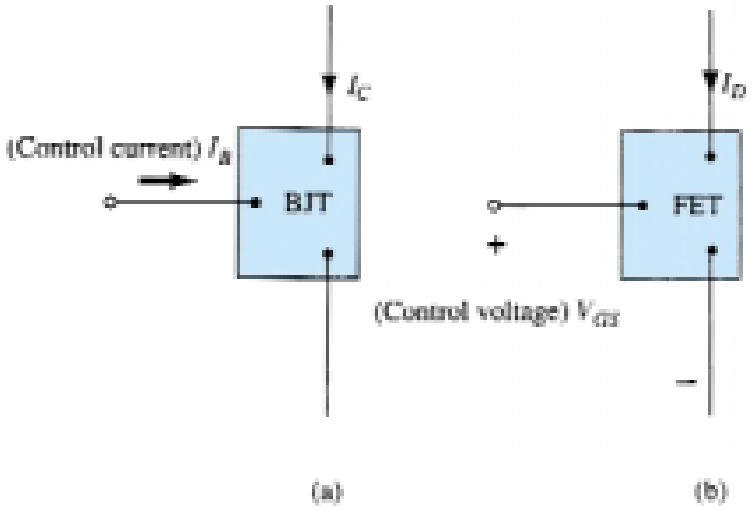


Fig. 7.7: (a) BJT and (b) FET

7.2.3 FET definition

FET is uni-polar device which means that the operation depends on only one type of charge carriers (*h* or *e)*. It is a Voltage controlled Device which means that the gate voltage controls drain current.

7.2.4 FET properties

FET have many advantages over than others transistors as the following:

- Unipolar device. Its operation depends on only one type of charge carriers (h or e)
- Voltage controlled Device (gate voltage controls drain current)
- Very high input impedance ($\approx 10^9$ - 10^{12} Ω)
- Source and drain are interchangeable in most Low-frequency applications
- Low Voltage Low Current Operation is possible (Low-power consumption)

- Less Noisy as Compared to BJT
- No minority carrier storage (Turn off is faster)
- Self limiting device
- Very small in size, occupies very small space in ICs
- Low voltage low current operation is possible in MOSFETS
- Zero temperature drift of output is possible

7.3 FET classification

Classification of FETs with their symbols can be shown in figure 7.8.

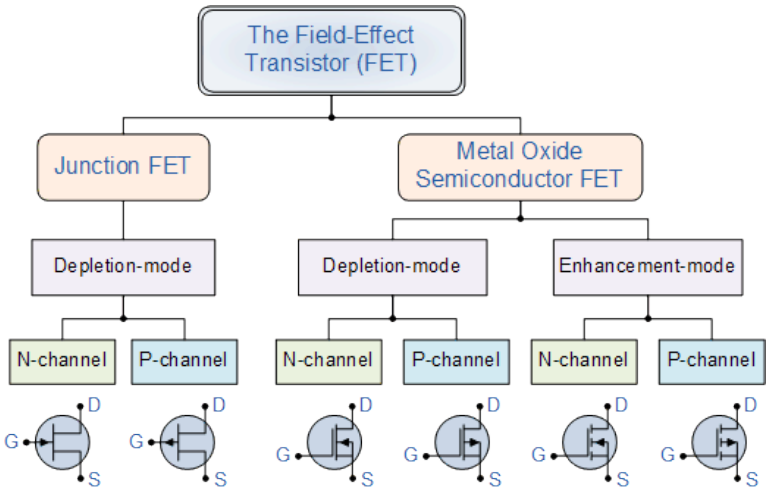


Fig. 7.8: Classification of FETs.

7.3.1 JFET

In this section, we will describe one of the most popular types in FET which is called Junction Field Effect Transistor (JFET).

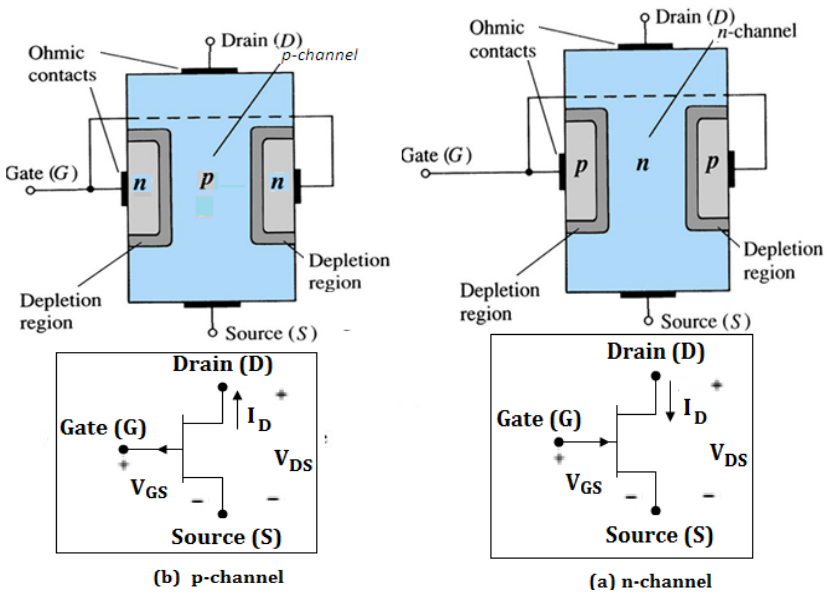


Fig. 7.9: JFETs.

The FET has three terminals which are called Gate (G), Drain (D) and Source (S).

As shown in figure 7.9, there are two types of JFETs. The n-channel is more widely used.

The basic construction of the n-channel JFET is shown in Fig. 7.9. Note that a major part of the structure is the n-type material that forms the channel between the embedded layers of p-type material. The top of the n-type channel is connected through an ohmic contact to a terminal referred to as the drain (D), while the lower end of the same material is connected through an ohmic contact to a terminal referred to as the source (S). The two p-type materials are connected together and to the gate (G) terminal. In essence, therefore, the drain and source are connected to the ends of the n-type channel and the gate to the two layers of p-type material. In the absence of any applied potentials the JFET has two p-n junctions under no-bias conditions. The result is a depletion region at each junction as shown in figure 7.9 that resembles the same region of a diode under no-bias conditions. Recall also that a depletion region is that region void of free carriers and therefore unable to support conduction through the region.

Analogies are seldom perfect and at times can be misleading, but the water analogy of figure 7.10 does provide a sense for the JFET control at the gate terminal and the appropriateness of the terminology applied to the terminals of the device. The source of water pressure can be likened to the applied voltage from drain to source that will

establish a flow of water (electrons) from the spigot (source). The "gate," through an applied signal (potential), controls the flow of water (charge) to the "drain".

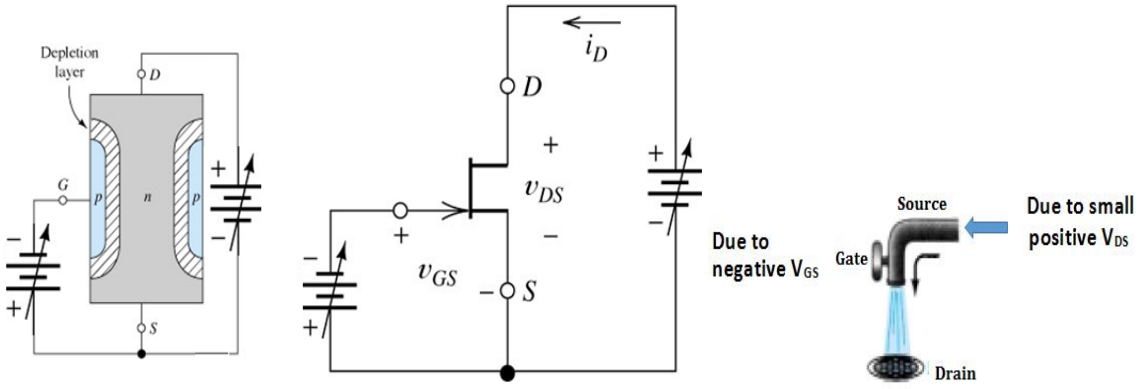


Fig. 7.10: N channel JFET.

The effect of V_{GS} is very important parameter. The following figure 7.9 shows the effect of varying V_{GS} with V_{DS}=0.

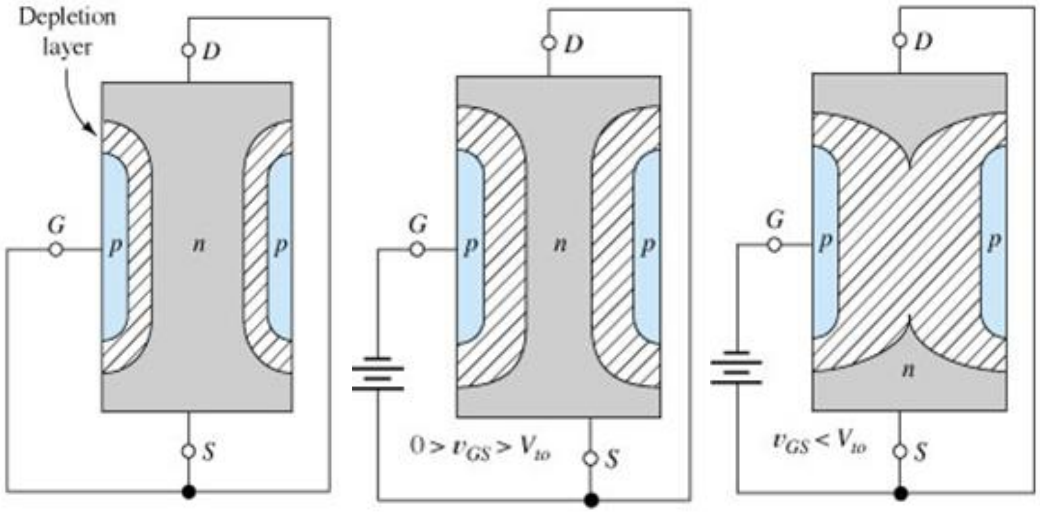


Fig. 7.11: The effect V_{GS}.

The operation of JFET will be described in details. As shown in figure 7.10 with V_{GS} = 0, and a small voltage (V_{DS}) applied between the Drain and the Source, maximum saturation current (I_{DSS}) will flow through the channel from the Drain to the Source restricted only by the small depletion region around the junctions. If a small negative

voltage ($-V_{GS}$) is now applied to the Gate the size of the depletion region begins to increase and therefore, reducing the overall effective area of the channel and thus reducing the current flowing through it. So by applying a reverse bias voltage increases the width of the depletion region which in turn reduces the conduction of the channel. Since the PN junction is reversed biased, little current will flow into the gate connection I_G=0. As the Gate voltage ($-V_{GS}$) is made more negative, the width of the channel decreases until no more current flows between the Drain and the Source and the FET is said to be "pinched-off" (similar to the cut-off region for a BJT). The voltage at which the channel closes is called the "pinch-off voltage", (V_P). In this pinch-off region the Gate voltage, VGS controls the channel current and VDS has little or no effect. The result is that the FET acts more like a voltage controlled resistor which has

- zero resistance when $\mathbf{V_{GS} = 0}$ and
- maximum "ON" resistance ($\mathbf{R_{DS}}$) when the **Gate voltage is very negative**

Under normal operating conditions, the JFET gate is always negatively biased relative to the source. Because a JFET is a voltage-controlled device, "NO current flows into the gate (I_G =0. Always GS is Reversed biased)" then the Source current (I_S) flowing out of the device equals the Drain current flowing into it and therefore ($I_D = I_S$).

The instant the voltage V_{DD} (= V_{DS}) is applied, the electrons will be drawn to the drain terminal, establishing the conventional current I_D. Where ($I_D = I_S$). The flow of charge is limited by the resistance of the *n*-channel between drain and source. As the voltage V_{DS} is increased from 0 to a few volts ($V_{DS} < V_P$) : the current will increase as determined by Ohm's law and the plot of I_D versus V_{DS} (Ohmic Region) . The relative straightness of the plot reveals that for the region of low values of V_{DS}, the resistance is essentially constant. As V_{DS} increases and approaches a level referred to as V_P, the depletion regions of will widen, causing a noticeable reduction in the channel width causes the resistance to increase. Leading to constant current_ with $V_{DS} > V_P$, the FET has the characteristics of a current source. If V_{DS} is increased to a level where it appears that the two depletion regions would "touch", a condition referred to as *pinch-off* will result. At the pinch-off point:

- Any further increase in V_{GS} does not produce any increase in I_D. V_{GS} at pinch-off is denoted as V_P.
- I_D is at saturation or maximum. It is referred to as I_{DSS}.

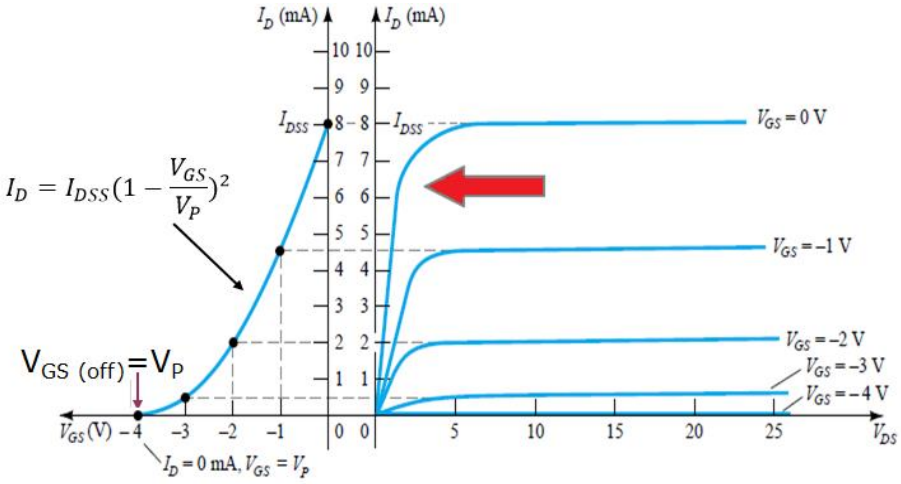
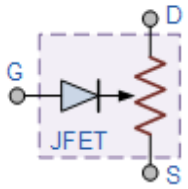


Fig. 7.12: The transfer characteristics curve for JFET.

The region to the left of the pinch-off point is called the *ohmic region*. The JFET can be used as a variable resistor, where V_{GS} controls the drain-source resistance (rd). As V_{GS} becomes more negative, the resistance (rd) increases

$$r_d = \frac{r_o}{\left(1 - \frac{V_{GS}}{V_P}\right)^2}$$



JFET Model

From this graph it is easy to determine the value of I_D for a given value of V_{GS} . It is also possible to determine I_{DSS} and V_P by looking at the knee where V_{GS} is 0.

The characteristics curves example in figure 7.13, shows the four different regions of operation for a JFET and these are given as:

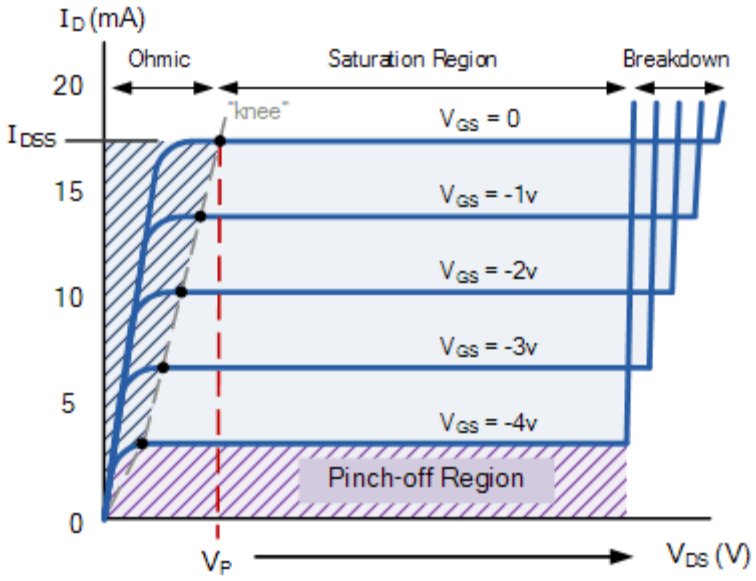


Fig.7.13: The characteristics curves for JFET.

- **Ohmic Region** – When **V_{GS} = 0** the depletion layer of the channel is **very small** and the JFET acts like **a voltage controlled resistor.**
- **Cut-off Region** – This is also known as the **pinch-off region** were the Gate voltage, **V_{GS}** is sufficient to cause the JFET to act as an **open circuit** as the channel
- **Saturation Region** – The JFET becomes a good conductor and is controlled by the Gate Source voltage, (V_{GS}) while the Drain-Source voltage, (V_{DS}) has little or no effect.
- **Breakdown Region** – The voltage between the Drain and the Source, (V_{DS}) is high enough to causes the JFET's resistive channel to break down and pass uncontrolled maximum current.

7.3.2 Depletion MOSFET

The basic construction of the *n*-channel depletion-type MOSFET is provided in Fig. 7.14.

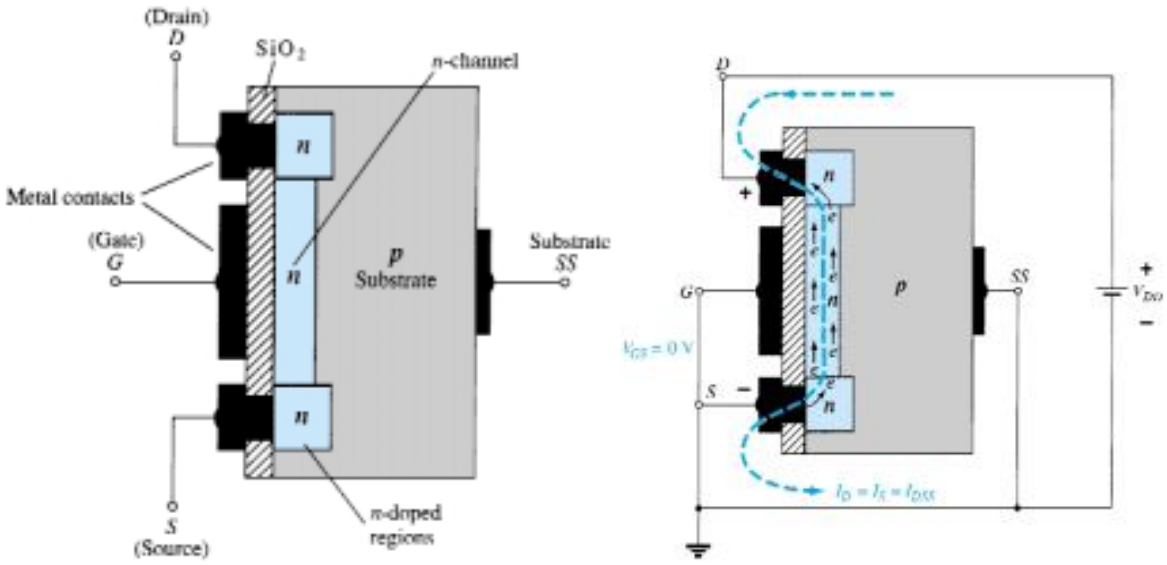


Fig. 7.14: The *n*-Channel depletion-type MOSFET.

A slab of p-type material is formed from a silicon base and is referred to as the substrate. It is the foundation upon which the device will be constructed. In some cases the substrate is internally connected to the source terminal. However, many discrete devices provide an additional terminal labeled SS, resulting in a four-terminal device, such as that appearing in Fig. 7.14. The source and drain terminals are connected through metallic contacts to n-doped regions linked by an n-channel as shown in the figure. The gate is also connected to a metal contact surface but remains insulated from the n-channel by a very thin silicon dioxide (SiO_2) layer. SiO_2 is a particular type of insulator referred to as a dielectric that sets up opposing (as revealed by the prefix di-) electric fields within the dielectric when exposed to an externally applied field. The fact that the SiO_2 layer is an insulating layer reveals the following fact:

- There is no direct electrical connection between the gate terminal and the channel of a MOSFET.

In addition:

- It is the insulating layer of SiO2 in the MOSFET construction that accounts for the very desirable high input impedance of the device.

In fact, the input resistance of a MOSFET is often that of the typical JFET, even though the input impedance of most JFETs is sufficiently high for most applications. The very high input impedance continues to fully support the fact that the gate current (I_G) is essentially zero amperes for dc-biased configurations. The reason for the label metal-oxide-semiconductor FET is now fairly obvious: metal for the drain, source, and gate connections to the proper surface—in particular, the gate terminal and the control to be offered by the surface area of the contact, the oxide for the silicon dioxide insulating layer, and the semiconductor for the basic structure on which the n- and p-type regions are diffused. The insulating layer between the gate and channel has resulted in another name for the device: insulated gate FET or IGFET, although this label is used less and less in current literature.

In Fig. 7.14 the gate-to-source voltage is set to zero volts by the direct connection from one terminal to the other, and a voltage VDS is applied across the drain-to-source terminals. The result is an attraction for the positive potential at the drain by the free electrons of the n-channel and a current similar to that established through the channel of the JFET. In fact, the resulting current with VGS = 0 V continues to be labeled ID_{SS}, as shown in Fig. 7.15.

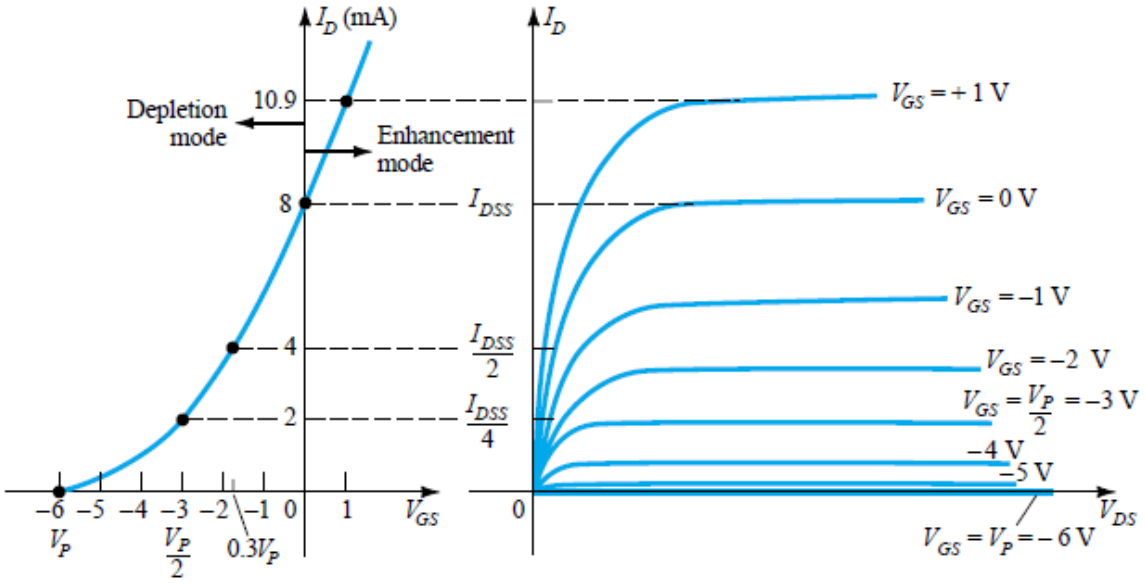


Fig. 7.15: The Drain and transfer characteristics for an n-channel depletion-type MOSFET.

In Fig. 7.16, V_{GS} has been set at a negative voltage such as -1 V. The negative potential at the gate will tend to pressure electrons toward the *p*-type substrate (like charges repel) and attract holes from the *p*-type substrate (opposite charges attract) as shown in Fig. 7.16.

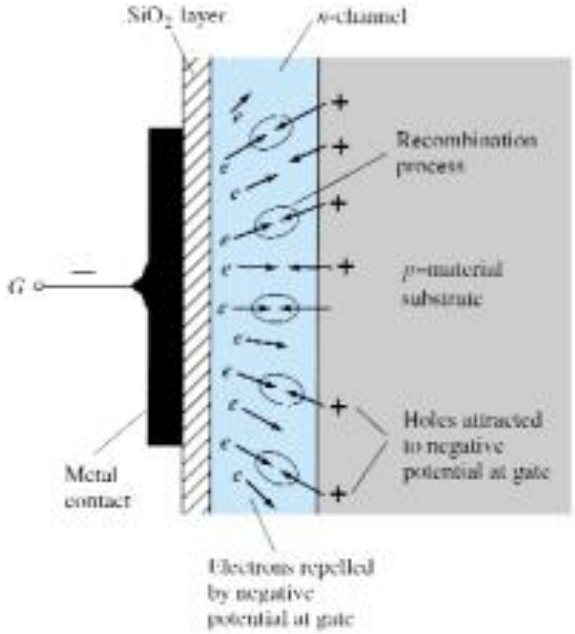


Fig. 7.16: Reduction in free carriers in channel due to a negative potential at the gate terminal.

Depending on the magnitude of the negative bias established by V_{GS}, a level of recombination between electrons and holes will occur that will reduce the number of free electrons in the *n*-channel available for conduction. The more negative the bias, the higher the rate of recombination. The resulting level of drain current is therefore reduced with increasing negative bias for V_{GS} as shown in Fig. 7.15 for V_{GS} = -1 V, -2 V, and so on, to the pinch-off level of -6 V. The resulting levels of drain current and the plotting of the transfer curve proceeds exactly as described for the JFET.

Finally, we can be seen the P-channel as shown in figure 7.17.

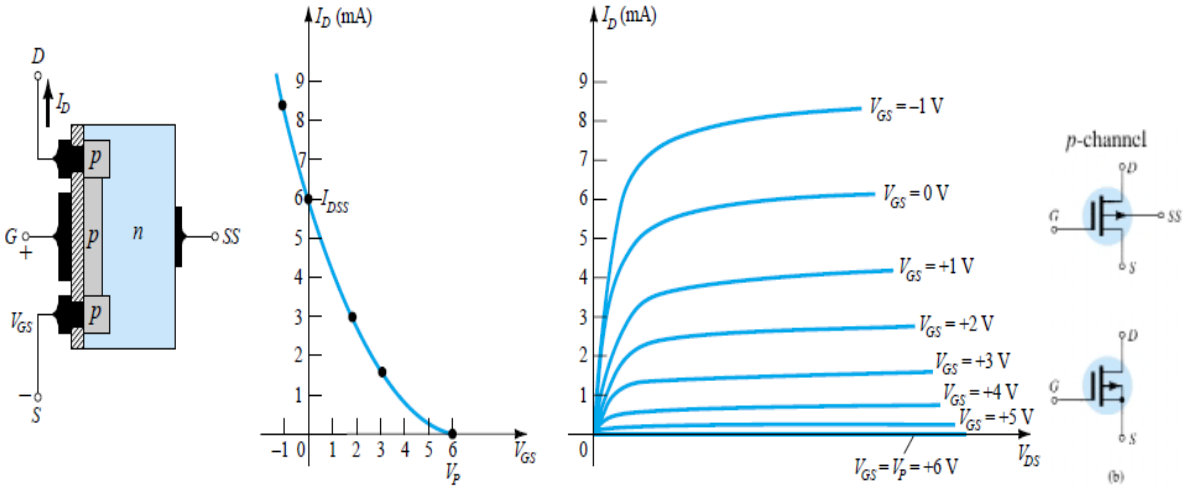


Fig. 7.17: P-channel depletion MOSFET

7.3.3 Enhancement MOSFET

The basic construction of the n-channel enhancement-type MOSFET is provided in Fig. 7.18. A slab of p-type material is formed from a silicon base and is again referred to as the substrate. As with the depletion-type MOSFET, the substrate is sometimes internally connected to the source terminal, while in other cases a fourth lead is made available for external control of its potential level. The source and drain terminals are again connected through metallic contacts to n-doped regions, but note in Fig. 7.18 the absence of a channel between the two n-doped regions. This is the primary difference between the construction of depletion-type and enhancement-type MOSFETs—the absence of a channel as a constructed component of the device. The SiO_2 layer is still present to isolate the gate metallic platform from the region between the drain and source, but now it is simply separated from a section of the p-type material. In summary, therefore, the construction of an enhancement-type MOSFET is quite similar to that of the depletion-type MOSFET, except for the absence of a channel between the drain and source terminals.

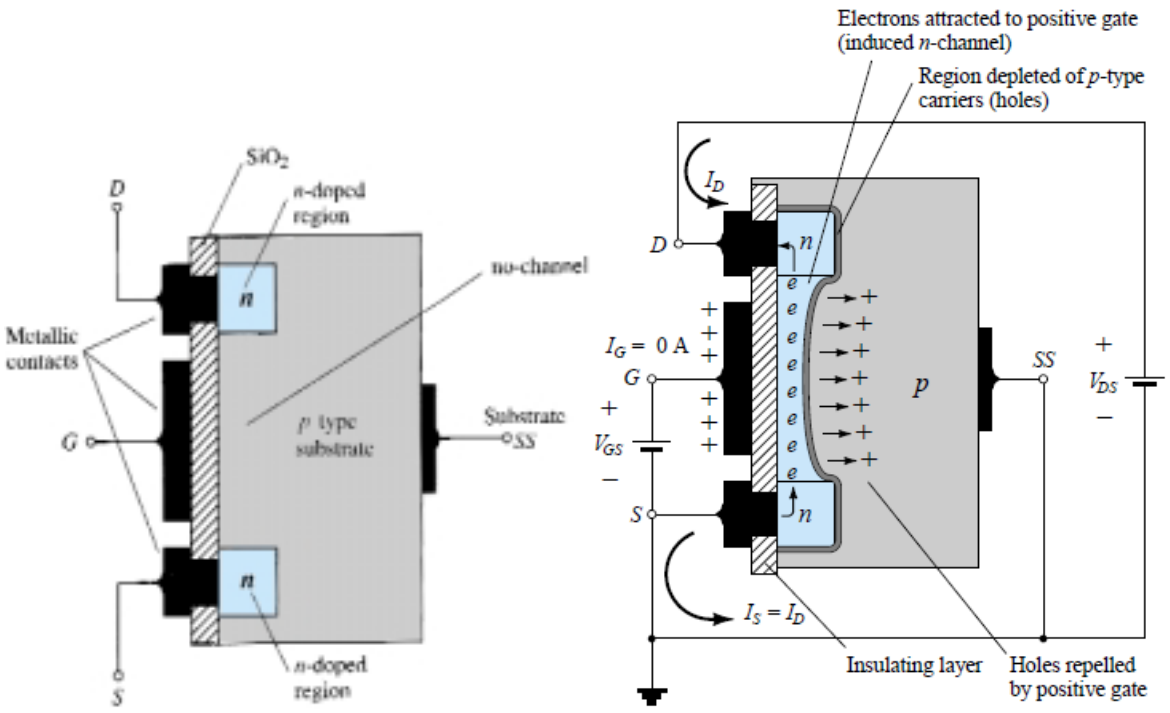


Fig. 7.18: The *n*-Channel enhancement type MOSFET.

If V_{GS} is set at 0 V and a voltage applied between the drain and source of the device of Fig. 7.18, the absence of an *n*-channel (with its generous number of free carriers) will result in a current of effectively zero amperes—quite different from the depletion- type MOSFET and JFET where $I_D = I_{DSS}$. It is not sufficient to have a large accumulation of carriers (electrons) at the drain and source (due to the *n*-doped regions) if a path fails to exist between the two. With V_{DS} some positive voltage, V_{GS} at 0 V, and terminal *SS* directly connected to the source, there are in fact two reverse-biased *p*-*n* junctions between the *n*-doped regions and the *p*-substrate to oppose any significant flow between drain and source.

In Fig. 7.18 both V_{DS} and V_{GS} have been set at some positive voltage greater than 0 V, establishing the drain and gate at a positive potential with respect to the source. The positive potential at the gate will pressure the holes (since like charges repel) in the *p*-substrate along the edge of the SiO_2 layer to leave the area and enter deeper regions of the *p*-substrate, as shown in the figure. The result is a depletion region near the SiO_2 insulating layer void of holes. However, the electrons in the *p*-substrate (the minority carriers of the material) will be attracted to the positive gate and accumulate in the region near the surface of the SiO_2 layer. The SiO_2 layer and its insulating qualities will prevent the negative carriers from being absorbed at the gate terminal. As V_{GS} increases in magnitude, the concentration of electrons near the SiO_2 surface increases

until eventually the induced *n*-type region can support a measurable flow between drain and source. The level of V_{GS} that results in the significant increase in drain current is called the *threshold voltage* and is given the symbol V_T. On specification sheets it is referred to as $V_{GS(Th)}$, although V_T is less unwieldy and will be used in the analysis to follow. Since the channel is nonexistent with V_{GS} = 0 V and "enhanced" by the application of a positive gate-to-source voltage, this type of MOSFET is called an *enhancement-type MOSFET*. Both depletion and enhancement type MOSFETs have enhancement type regions, but the label was applied to the latter since it is its only mode of operation.

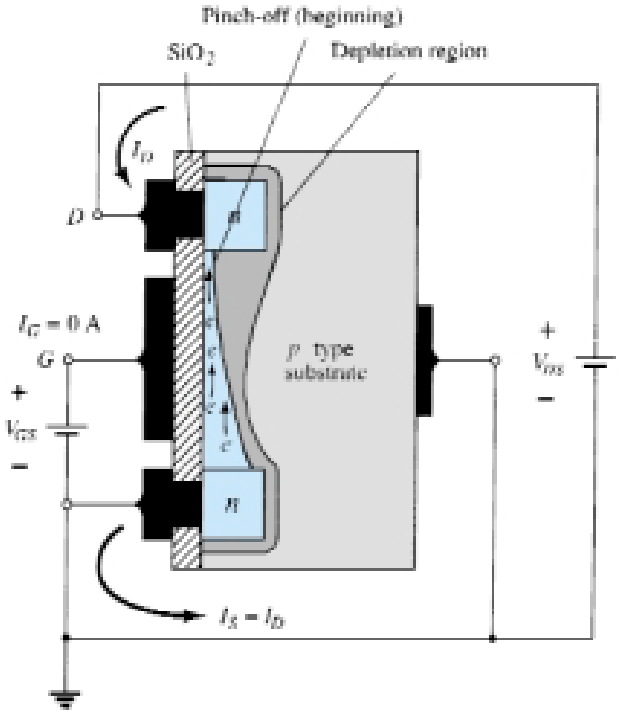


Fig. 7.19: Change in channel and depletion region

As V_{GS} is increased beyond the threshold level, the density of free carriers in the induced channel will increase, resulting in an increased level of drain current. However, if we hold V_{GS} constant and increase the level of V_{DS}, the drain current will eventually reach a saturation level as occurred for the JFET and depletion-type MOSFET. The leveling off of I_D is due to a pinching-off process depicted by the narrower channel at the drain end of the induced channel as shown in Fig. 7.19. Applying Kirchhoff's voltage law to the terminal voltages of the MOSFET of Fig. 7.19, we find that

$$V_{DG} = V_{DS} - V_{GS}$$

If V_{GS} is held fixed at some value such as 8 V and V_{DS} is increased from 2 to 5 V, the voltage V_{DG} will drop from -6 to -3 V and the gate will become less and less positive with respect to the drain. This reduction in gate-to-drain voltage will in turn reduce the attractive forces for free carriers (electrons) in this region of the induced channel, causing a reduction in the effective channel width. Eventually, the channel will be reduced to the point of pinch-off and a saturation condition will be established as described earlier for the JFET and depletion-type MOSFET. In other words, any further increase in V_{DS} at the fixed value of V_{GS} will not affect the saturation level of I_D until breakdown conditions are encountered. The drain characteristics of Fig. 7.20 reveal that for the device of Fig. 7.19 with V_{GS} = 8 V, saturation occurred at a level of V_{DS} = 6 V. In fact, the saturation level for V_{DS} is related to the level of applied V_{GS} by

$$V_{DS_{sat}} = V_{GS} - V_T$$

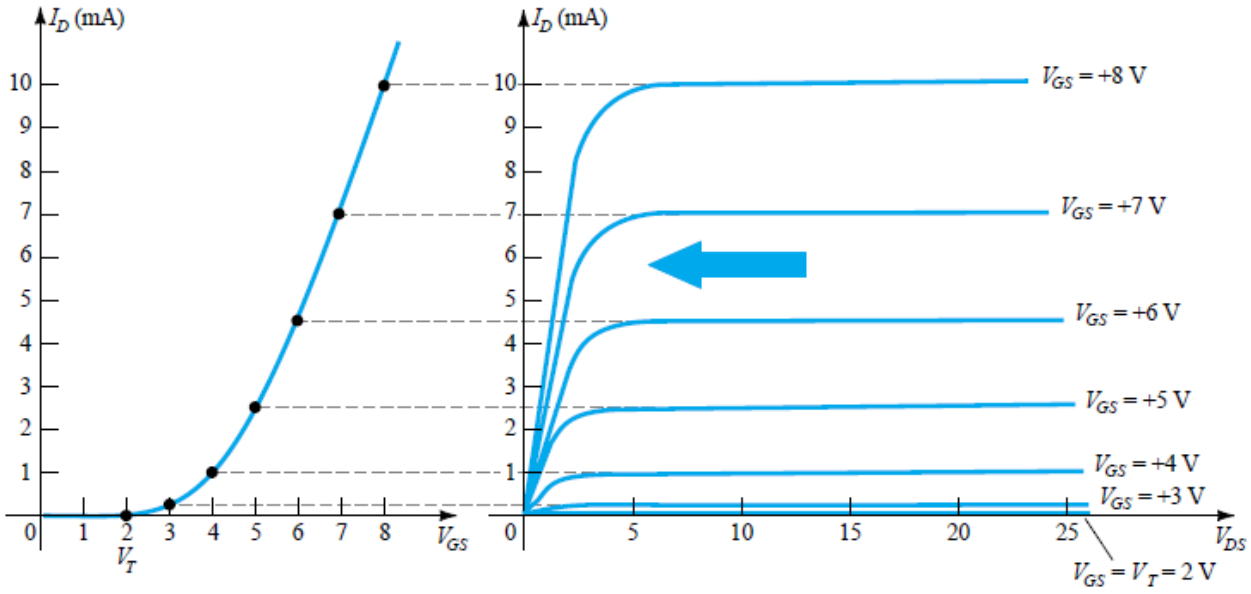


Fig. 7.20: The characteristics for an n-channel enhancement type MOSFET

Obviously, therefore, for a fixed value of V_T, then the higher the level of V_{GS}, the more the saturation level for V_{DS}, as shown in Fig. 7.19 by the locus of saturation levels. For the characteristics of Fig. 7.19 the level of V_T is 2 V, as revealed by the fact that the drain current has dropped to 0 mA. In general, therefore:

- For values of V_{GS} less than the threshold level, the drain current of an enhancement type MOSFET is 0 mA.

Figure 7.20 clearly reveals that as the level of V_{GS} increased from V_T to 8 V, the resulting saturation level for I_D also increased from a level of 0 to 10 mA. In addition, it is quite noticeable that the spacing between the levels of V_{GS} increased as the magnitude of V_{GS} increased, resulting in ever-increasing increments in drain current. For levels of $V_{GS} = V_T$, the drain current is related to the applied gate-to-source voltage by the following nonlinear relationship:

$$I_D = k(V_{GS} - V_T)^2$$

Again, it is the squared term that results in the nonlinear (curved) relationship between I_D and V_{GS}. The k term is a constant that is a function of the construction of the device. The value of k can be determined from the following equation where I_D (on) and V_{GS} (on) are the values for each at a particular point on the characteristics of the device.

$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_T)^2}$$

Substituting I_D(on) = 10 mA when V_{GS}(on) = 8 V from the characteristics of Fig. 7.20 yields

$$K = 0.278 \text{ mA/V}^2$$

Finally, we can be seen the P-channel as shown in figure 7.21.

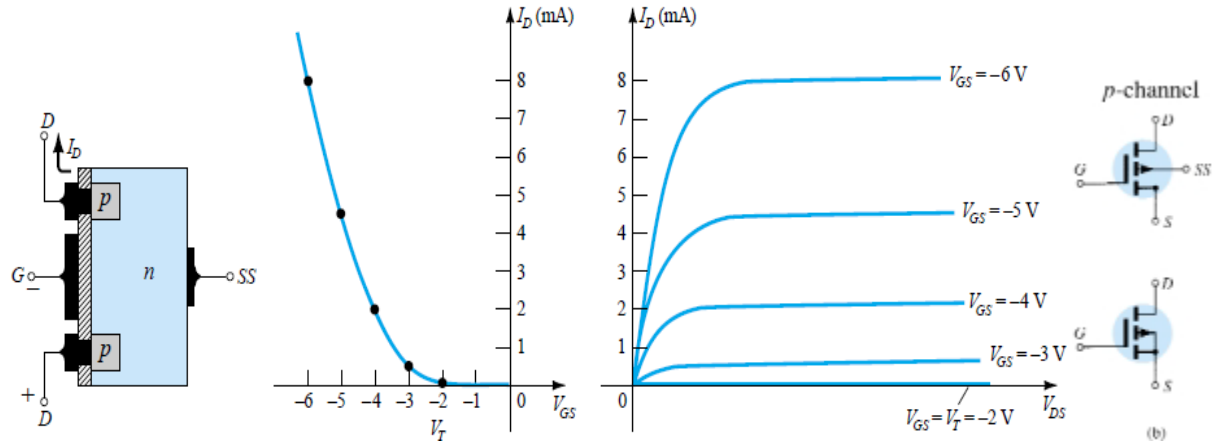


Fig. 7.21: P-channel enhancement MOSFET

7.4 DC analysis for FET

For the field-effect transistor, the relationship between input and output quantities is nonlinear due to the squared term in Shockley's equation. Linear relationships result in straight lines when plotted on a graph of one variable versus the other, while nonlinear functions result in curves as obtained for the transfer characteristics of a JFET. The nonlinear relationship between I_D and V_{GS} can complicate the mathematical approach to the dc analysis of FET configurations. A graphical approach may limit solutions to tenths-place accuracy, but it is a quicker method for most FET amplifiers. Since the graphical approach is in general the most popular, the analysis of this chapter will have a graphical orientation rather than direct mathematical techniques. Another distinct difference between the analysis of BJT and FET transistors is that the input controlling variable for a BJT transistor is a current level, while for the FET a voltage is the controlling variable. In both cases, however, the controlled variable on the output side is a current level that also defines the important voltage levels of the output circuit. The general relationships that can be applied to the dc analysis of all FET amplifiers are

$$I_G \cong 0 \text{ A} \qquad I_D = I_S$$

For JFETS and depletion-type MOSFETs, Shockley's equation is applied to relate the input and output quantities:

$$I_D = I_{DSS}\left(\frac{1 - V_{GS}}{V_P}\right)^2$$

For enhancement-type MOSFETs, the following equation is applicable:

$$I_D = k(V_{GS} - V_T)^2$$

7.5 AC analysis for FET

Field-effect transistor amplifiers provide an excellent voltage gain with the added feature of a high input impedance. They are also considered low-power consumption configurations with good frequency range and minimal size and weight. Both JFET and depletion MOSFET devices can be used to design amplifiers having similar voltage gains. The depletion MOSFET circuit, however, has a much higher input impedance than a similar JFET configuration.

While a BJT device controls a large output (collector) current by means of a relatively small input (base) current, the FET device controls an output (drain) current by means of a small input (gate-voltage) voltage. In general, therefore, the BJT is a current-controlled device and the FET is a voltage-controlled device. In both cases, however, note that the output current is the controlled variable. Because of the high input characteristic of FETs, the ac equivalent model is somewhat simpler than that employed for BJTs. While the BJT had an amplification factor β (beta), the FET has a trans-conductance factor, g_m.

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

$$g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{Q\text{-pt.}} = \left.\frac{dI_D}{dV_{GS}}\right|_{Q\text{-pt.}} = \frac{d}{dV_{GS}}\left[I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2\right]$$

$$= I_{DSS}\frac{d}{dV_{GS}}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 2I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]\frac{d}{dV_{GS}}\left(1 - \frac{V_{GS}}{V_P}\right)$$

$$= 2I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]\left[\frac{d}{dV_{GS}}(1) - \frac{1}{V_P}\frac{dV_{GS}}{dV_{GS}}\right] = 2I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]\left[0 - \frac{1}{V_P}\right]$$

$$g_m = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{V_{GS}}{V_P}\right]$$

$$g_{m0} = \frac{2I_{DSS}}{|V_P|}$$

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right]$$

7.6 FET small signal model

The input impedance of all commercially available FETs is sufficiently large to assume that the input terminals approximate an open circuit. In equation form,

$$Z_i\ (\text{FET}) = \infty\ \Omega$$

The output impedance of FETs is similar in magnitude to that of conventional BJTs. On FET specification sheets, the output impedance will typically appear as y_{os}.

$$Z_o\,(\text{FET}) = r_d = \frac{1}{y_{os}} \qquad r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}=\text{constant}}$$

As shown in this figure 7.22, the FET AC equivalent circuit.

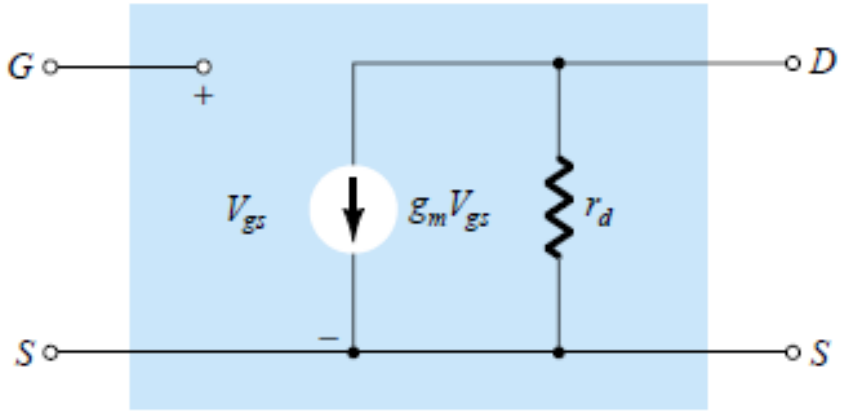


Fig. 7.22: FET AC equivalent circuit

7.7 Sheet 7

1. Describe the BJT?
2. Discuss by graph construction, modeling and symbols for BJT?
3. How is the BJT working as amplifier?
4. State the modes of operation for BJT?
5. How is the BJT working as the switch?
6. Describe in details collector characteristics curve?
7. State the types of biasing circuits?
8. Draw each of the following:
   - The basic construction of a *n*-channel JFET.
   - The basic construction of a *n*-channel depletion MOSFET.
   - The basic construction of a *n*-channel enhancement MOSFET.
   - The basic construction of a *p*-channel JFET.
   - The basic construction of a *p*-channel depletion MOSFET.
   - The basic construction of a *p*-channel enhancement MOSFET.
   - The basic construction of a *CMOS*.

9. Describe in details the operation for each of the following:
   - a *n*-channel JFET
   - a *n*-channel depletion MOSFET.
   - a *n*-channel enhancement MOSFET.

Chapter 8

Operational Amplifier (OPAMP)

Chapter 8

Operational Amplifier (OPAMP)

8.1 Introduction

Operational amplifier (Op-amp) is made of many transistors, diodes, resistors, and capacitors in integrated circuit technology. An op-amp is a "differential-to-single-ended" amplifier, i.e., it amplifies the voltage difference $V_p - V_n = V_i$ at the input port and produces a voltage Vo at the output port that is referenced to the ground node of the circuit in which the op-amp is used as shown in Fig. 8.1.

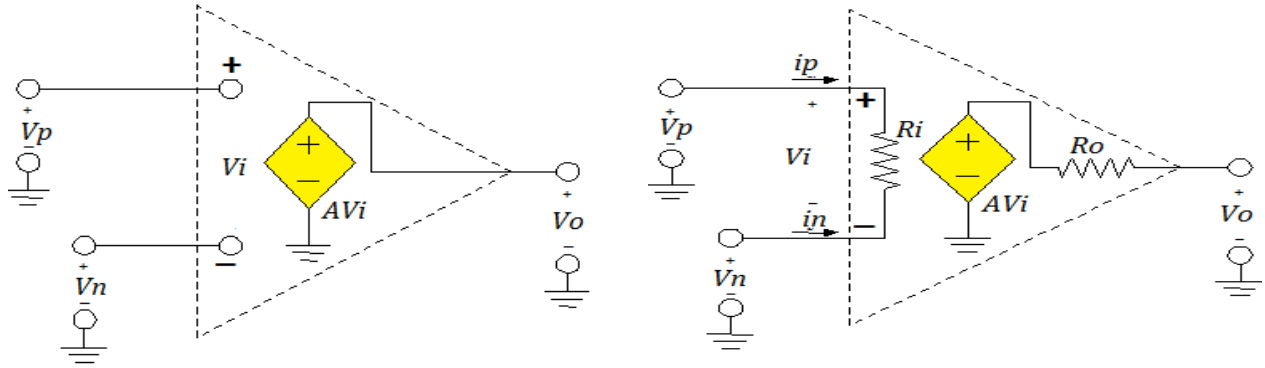


Fig. 8.1: Ideal and standard OPAMP.

Common Operational Amplifier Common Mode and Differential Mode Input is shown in the following equations:

$$A_{ud} = \frac{v_{od}}{v_{id}} \qquad K_{CMR} = \left|\frac{A_{ud}}{A_{uc}}\right|$$

$$A_{uc} = \frac{v_{oc}}{v_{ic}} \qquad K_{CMR} = 20\log\left|\frac{A_{ud}}{A_{uc}}\right| \quad (\text{dB})$$

$$V_d = V_{i_1} - V_{i_2} \qquad V_c = \tfrac{1}{2}(V_{i_1} + V_{i_2})$$

$$V_o = A_d V_d + A_c V_c \qquad \text{CMRR} = \frac{A_d}{A_c}$$

$$\text{CMRR (log)} = 20 \log_{10} \frac{A_d}{A_c} \quad \text{(dB)}$$

It has five terminals as shown in Fig. 8.2:

- non-inverting input (Vp): The input terminal marked with a "+"
- Inverting input (Vn): the input terminal marked with a "–"
- Output terminal
- +ve supply terminal
- -ve or ground supply terminal

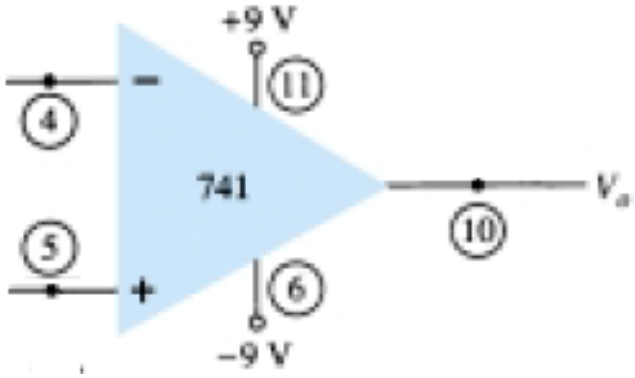


Fig. 8.2: Terminals of OPAMP.

8.2 Properties of OPAMP

Characteristics of Ideal OPAMP are shown below as shown in Fig. 8.3:

- Gain is infinite: $A = \infty$
- Input resistance is infinite: $R_i = \infty$
- Output resistance is zero: $R_o = 0$
- Infinite frequency bandwidth

- $V_p = V_n$
- $i_n = i_p = 0$

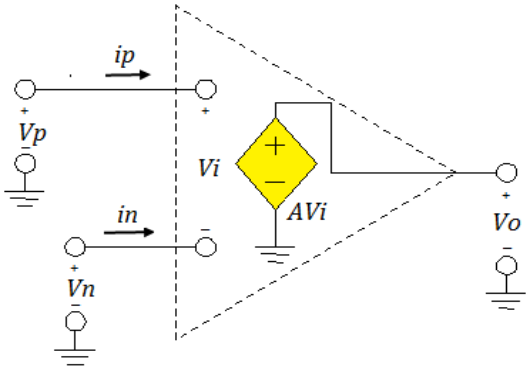


Fig. 8.3: Characteristics of Ideal OPAMP.

8.3 OPAMP applications

OPAMP was used in many applications such as:

- Non-Inverting Amplifier

Fig. 8.4 shows circuit, all equations, and relations for this type.

$$V_{in} = \frac{V_{out}}{R_1 + R_f} * R_1 \quad V_{out} = (1 + \frac{R_f}{R_1}) * V_{in}$$

$$A = \frac{V_{out}}{V_{in}} = (1 + \frac{R_f}{R_1}) \geq 1$$

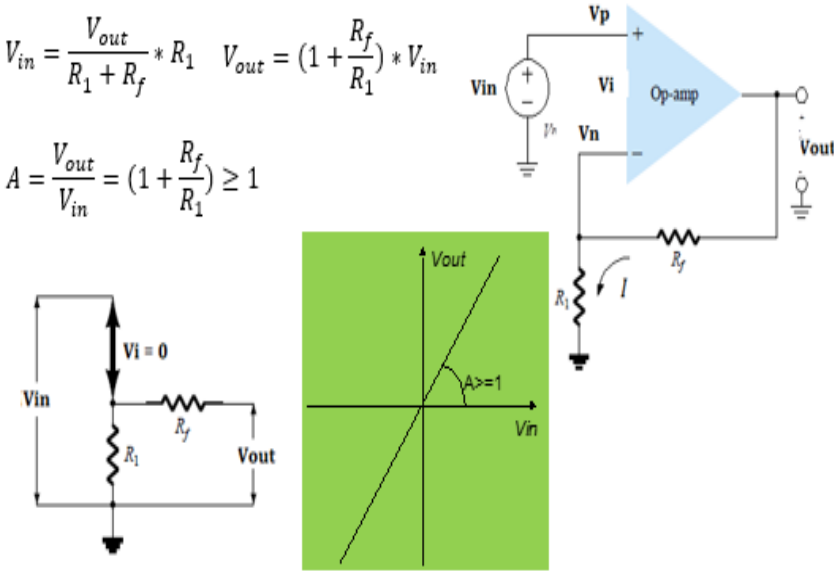
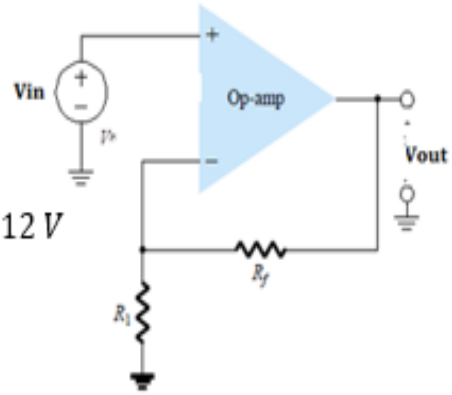


Fig. 8.4: Non-Inverting Amplifier

Example 8.1:

Calculate the output voltage and the voltage gain (in dB) of a noninverting amplifier for values of V_{in} = 2 V, R_f = 500 kΩ, and R_1 = 100 k Ω.



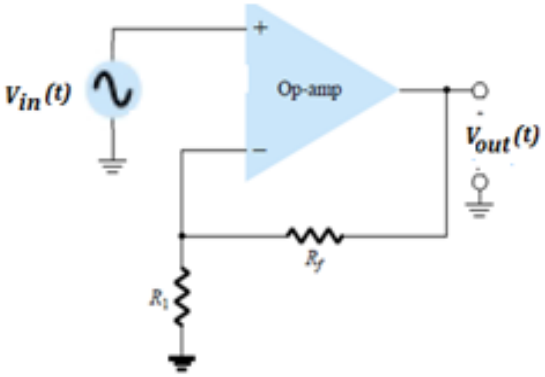
Solution

$$V_{out} = \left(1 + \frac{R_f}{R_1}\right) * V_{in} = \left(1 + \frac{500\ K\Omega}{100\ K\Omega}\right) * 2\ V = +12\ V$$

$$G_{V(dB)} = 20\ log\left(\frac{V_{out}}{V_{in}}\right) = 20\ log\left(\frac{12\ V}{2\ V}\right) = 20 \log 6 = 15.563\ dB$$

Example 8.2:

Calculate the output voltage from the circuit shown in Figure for an input of $V_{in}(t) = 120\ sin(wt)\ uV$, R_f = 240 KΩ and R_1 = 2.4 :KΩ.



Solution

$$G = \frac{V_{out}}{V_{in}} = \left(1 + \frac{R_f}{R_1}\right) = 1 + 100 = 101$$

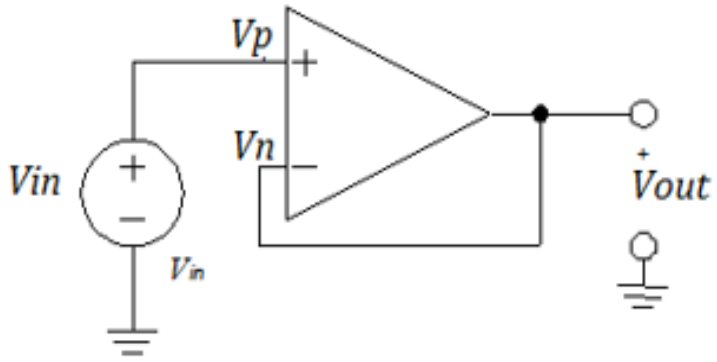
$$V_{out} = G * V_{in} = 101 * 120 \sin(wt) = 12.12\ \sin(wt)\ mV$$

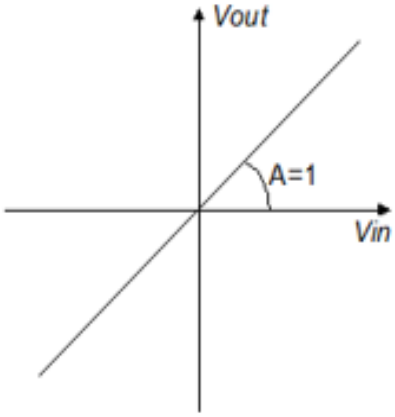
Example 8.3:

application: Unity Voltage Follower (Voltage buffer)

$V_{out} = V_{in}$

$A = 1$





- Inverting Amplifier

Fig. 8.5 shows circuit, all equations, and relations for this type.

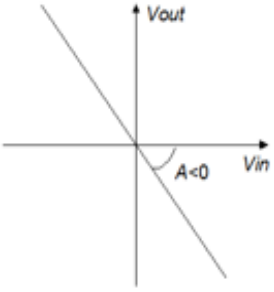
Apply KCL

$\frac{V_n - V_{in}}{R_1} = \frac{V_{out} - V_n}{R_f}$

Since $V_n = 0$, we have:

$\frac{V_{out}}{R_f} = \frac{-V_{in}}{R_1}$

$\frac{V_{out}}{V_{in}} = A = \frac{-R_f}{R_1}$



Voltage transfer curve of inverting amplifier

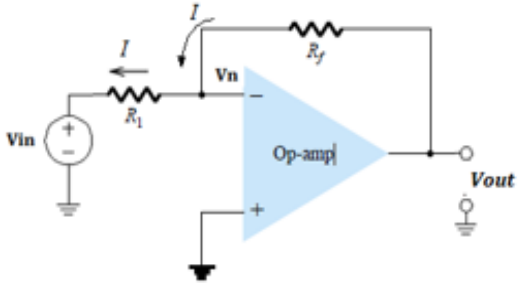


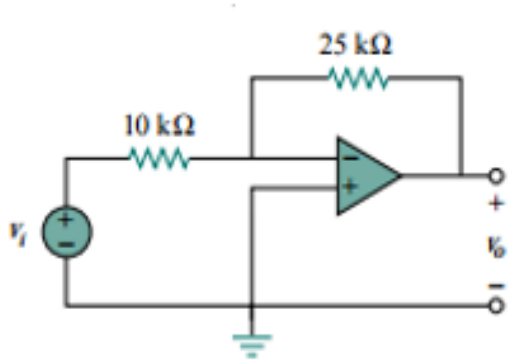
Fig. 8.5: Inverting Amplifier

Example 8.4:

Refer to the op amp in the following figure. If Vi = 0.5 V, calculate

a) The output voltage Vo

b) The current in the 10 K ohm resistor



(a)

$$\frac{v_o}{v_i} = -\frac{R_f}{R_1} = -\frac{25}{10} = -2.5$$

$$v_o = -2.5v_i = -2.5(0.5) = -1.25 \text{ V}$$

(b) The current through the 10-kΩ resistor is

$$i = \frac{v_i - 0}{R_1} = \frac{0.5 - 0}{10 \times 10^3} = 50\ \mu\text{A}$$

- Summing Amplifier

Fig. 8.6 shows circuit, all equations, and relations for this type.

$$V_o = -i_F * R_F$$

Since v_i=0

$$i_F = i_A + i_B = \frac{V_A}{R_A} + \frac{V_B}{R_B}$$

$$V_o = -R_F * \left(\frac{V_A}{R_A} + \frac{V_B}{R_B}\right)$$

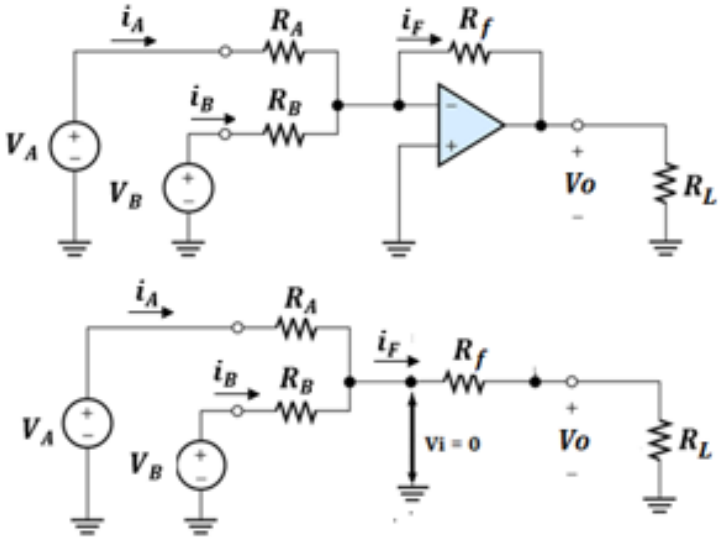
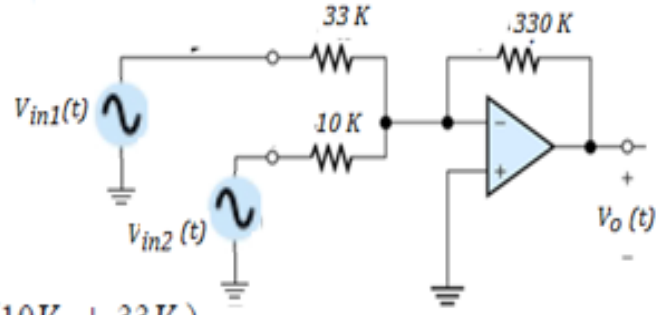


Fig. 8.6: Summing Amplifier

Example 8.5:

Calculate the output voltage for the following circuit . The inputs are $V_{in1} = 50\sin(1000t)$ mV and $V_{in2} = 10\sin(3000t)$ mV.

Solution



$$V_o = -\left(\frac{330\ \text{k}\Omega}{33\ \text{k}\Omega}V_1 + \frac{330\ \text{k}\Omega}{10\ \text{k}\Omega}V_2\right) = -(10V_1 + 33V_2)$$

$$= -[10(50\ \text{mV})\sin(1000t) + 33(10\ \text{mV})\sin(3000t)]$$

$$= \mathbf{-[0.5\sin(1000t) + 0.33\sin(3000t)]}$$

- Subtractor Amplifier

Fig. 8.7 shows circuit, all equations, and relations for this type.

$$V_o = \frac{R_3}{R_1 + R_3}\frac{R_2 + R_4}{R_2}V_1 - \frac{R_4}{R_2}V_2$$

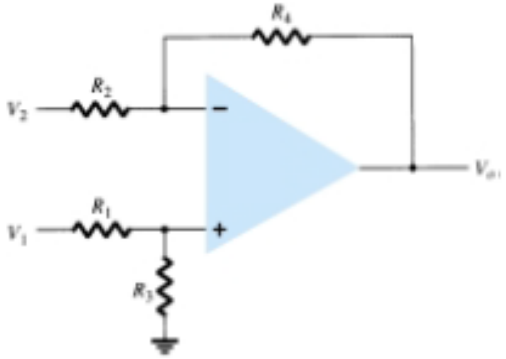
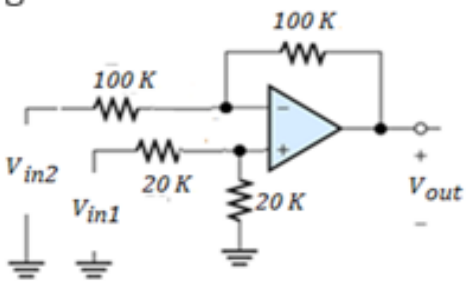


Fig. 8.7: Subtractor Amplifier

Example 8.6:

Determine the output voltage for the following circuit

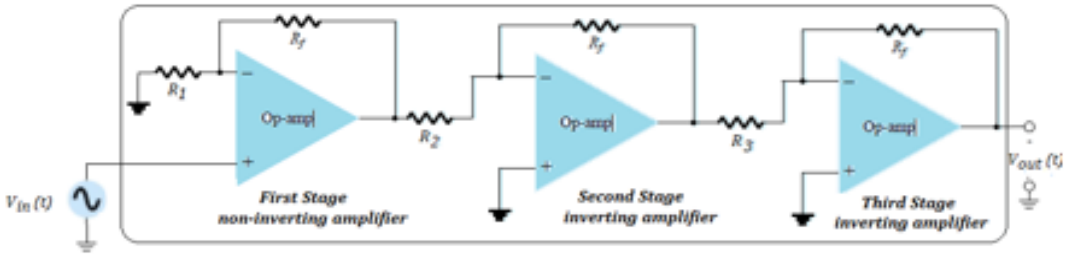
Solution



$$V_o = \left(\frac{20\ \text{k}\Omega}{20\ \text{k}\Omega + 20\ \text{k}\Omega}\right)\left(\frac{100\ \text{k}\Omega + 100\ \text{k}\Omega}{100\ \text{k}\Omega}\right) V_1 - \frac{100\ \text{k}\Omega}{100\ \text{k}\Omega} V_2$$
$$= V_1 - V_2$$

- Multiple-Stage Gains

Fig. 8.8 shows circuit, all equations, and relations for this type.



The figure shows an amplifier with three stages.

- The first stage is connected to provide noninverting gain.
- The next two stages provide an inverting gain .

$$G_1 = 1 + \frac{R_f}{R_1} \qquad G_2 = -\frac{R_f}{R_2} \qquad G_3 = -\frac{R_f}{R_3} \qquad \boldsymbol{G = G_1 G_2 G_3}$$

Fig. 8.8: Multiple-Stage

Example 8.7:

An LM124 quad op-amp is used as a three-stage amplifier.

a) Calculate the output voltage for resistor components of value

R_f =470 kΩ R_1= 4.3 kΩ, R_2 = 33 kΩ, and R_3 = 33 kΩ for an input of

80 sin(wt) uV.

b) Design the a three-stage amplifier for the individual gains of 10, -18 and -27 using feedback resistor of 270 KΩ

Solution

A) The amplifier gain $G = G_1G_2G_3 = \left(1 + \frac{R_f}{R_1}\right)\left(-\frac{R_f}{R_2}\right)\left(\frac{R_f}{R_3}\right)$

$$G = G_1G_2G_3 = \left(1 + \frac{470\ K\Omega}{4.3\ K\Omega}\right)\left(-\frac{470\ K\Omega}{33\ K\Omega}\right)\left(-\frac{470\ K\Omega}{33\ K\Omega}\right) = 22.2 * 10^3$$

$$V_o(t) = G * V_{in}(t) = 22.2 * 10^3 * 80\sin(wt)\ uV = 1.78\sin(wt)\ V$$

b) Design of the three stages amplifier

$$G_1 = 1 + \frac{R_f}{R_1} = 1 + \frac{R_f}{R_1} = +10 \qquad \frac{R_f}{R_1} = 9 = \frac{270\ K\Omega}{R_1} \quad R_1 = 30\ K\Omega$$

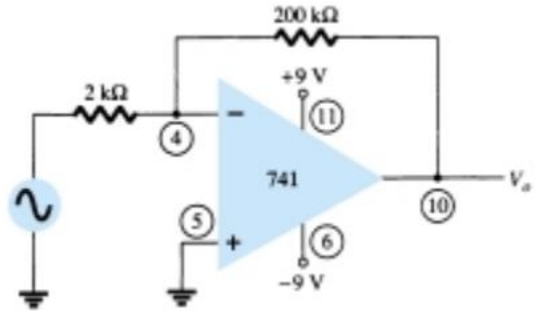
$$G_2 = -\frac{R_f}{R_2} = -\frac{270\ K\Omega}{R_2} = -18 \qquad R_2 = 15\ K\Omega$$

$$G_3 = -\frac{R_f}{R_3} = -\frac{270\ K\Omega}{R_3} = -27 \qquad R_3 = 10\ K\Omega$$

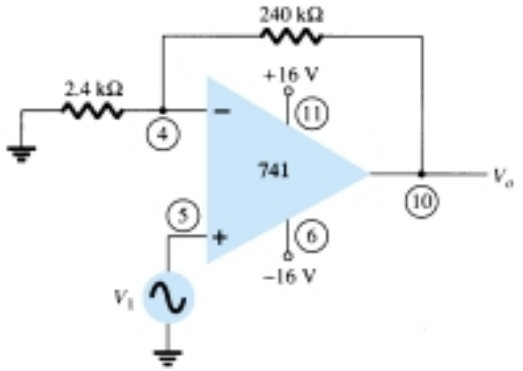
8.4 Sheet 8

1. Describe in detail the OPAMP?

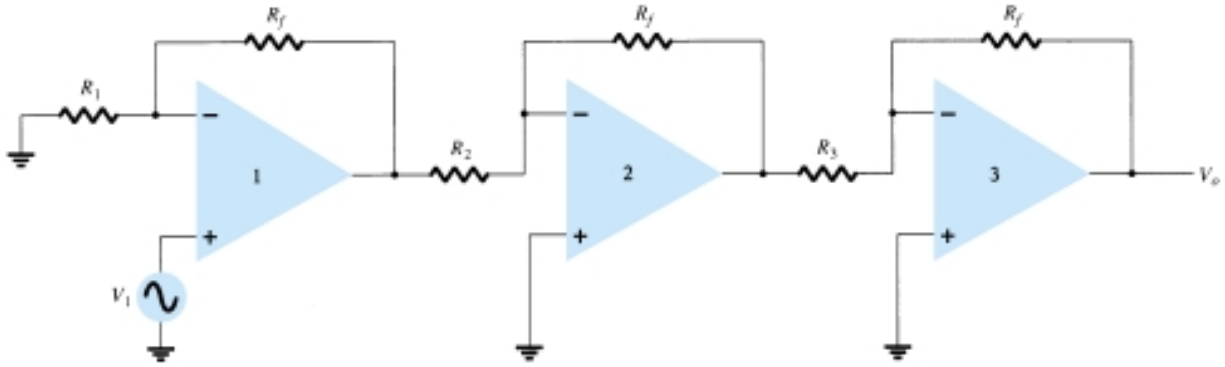
2. Determine the output voltage for the circuit of the following Fig. with a sinusoidal input of 2.5 mV



3. Calculate the output voltage from the circuit of the following Fig. for an input of 120 V.



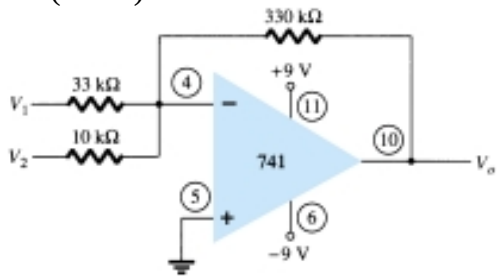
4. Calculate the output voltage using the circuit of the following Fig. for resistor components of value Rf = 470 k, R1 = 4.3 k, R2 = 33 k, and R3 = 33 k for an input of 80 µV.



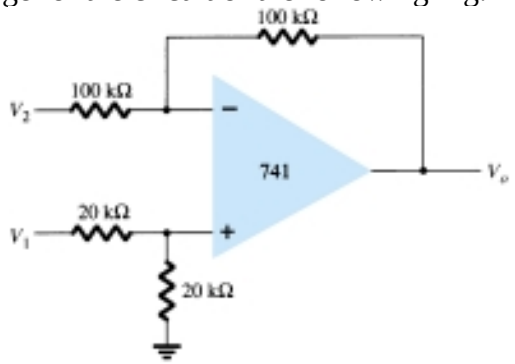
5. Show the connection of an LM124 quad op-amp as a three-stage amplifier with gains of 10, 18, and 27. Use a 270-k feedback resistor for all three circuits. What output voltage will result for an input of 150 V?

6. Show the connection of three op-amp stages using an LM348 IC to provide outputs that are 10, 20, and 50 times larger than the input. Use a feedback resistor of Rf 500 k in all stages

7. Calculate the output voltage for the circuit of the following Fig. The inputs are V1 = 50 mV sin(1000t) and V2 = 10 mV sin(3000t).



8. Determine the output voltage for the circuit of the following Fig.



lab

Choose any problem and make it by using any electronic simulator.

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[7] https://slideplayer.com/slide/9420623/